Interference-Aware Integration of Mixed-Signal Designs and Ultra High Voltage Pulse Generators for System-on-Chips

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genehmigte Dissertation von M.Sc. Katrin Gertrud Hirmer aus Bad Säckingen
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2. Gutachten: Prof. Dr.-Ing. Dirk Killat

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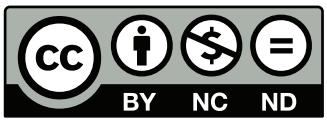

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Darmstadt, 25. Oktober 2019

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Katrin Hirmer

Acknowledgment

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With the submission of this work, another chapter of my life is written. The journey continues now — I have many plans and dreams. I thank everyone mentioned here, they will always be part of my journey. And I already thank all those who will join in the further journey.

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Katrin Hirmer

Abstract

The interference-aware implementation of system-on-chips (SoCs) including ultra high voltage pulse generators and mixed-signal devices, which are for example used in rectifiers or gate drivers, enables the continuous miniaturization of system electronics. Square wave signals with high amplitudes and slew rates can interfere significantly with monolithically integrated low voltage electronics. The prediction of these interferences on SoCs prior to fabrication is essential to take countermeasures. This helps to ensure the functionality of the system and reduces development costs.

The main objective of this work is to develop a model which can predict the influences of high voltage pulses on circuits with low supply voltages by simulations. The integration of this model into the conventional design flow of integrated circuits enables SPICE simulations without any additional license fees. The investigations within this thesis allow deriving recommendations for the integration of high voltage pulses and low voltage circuitry within a SoC.

Two SoCs have been fabricated in a silicon-on-insulator process. These can be used to emit light from an electroluminescent device as well as driving a capacitive sensor at the same time. The implemented ultra high voltage pulse generator can deliver pulses with up to ±300 V at slew rates of up to 99.56 $V\mu s^{-1}$. It is able to drive capacitive loads of 10 nF at frequencies of up to 5 kHz. At the same time, a spread spectrum clock generator (SSCG) with a resolution of 9 bit can excite the capacitive sensor with a bandwidth of 10.14 MHz and an attenuation of 33.17 dB with a 5 V power supply.

During the switching operation of the ultra high voltage pulse generator, deviations of the operating frequency of the SSCG can be observed. These can mostly be explained by substrate coupling. To verify the coupling mechanism, on the one hand, relevant impedances of the substrate network are measured and compared to calculated values within this thesis. On the other hand, the coupling of the high voltage pulse generator to the substrate as well as the influences of variations of the substrate potential on low voltage designs are recorded by measurement.

To predict the interferences on mixed-signal devices, a substrate netlist can be extracted with the help of the SoC layout. The parameters of the components within the substrate equivalent circuit can be analytically calculated by using geometric dimensions extracted from the layout of the SoC. The substrate netlist can be simulated along with the post-layout of the integrated components. The modeling of the supply voltage as well as the packaging is of great importance for the simulation. The investigations of this thesis result in recommendations for the implementation of SoCs with ultra high voltage pulse generators and mixed-signal devices. They include considerations for the circuit implementation, the layout as well as the package selection. For the fabricated SoCs, the frequency change of the SSCG can be reduced by 77.35 %.

Kurzfassung

Die störungsfreie Implementierung von System-on-Chips (SoCs) mit integrierten Ultra-Hochvolt-Pulsquellen und Mixed-Signal Schaltungen, wie sie beispielsweise in Gleichrichtern und Gate-Treibern eingesetzt werden, ermöglicht die stetige Verkleinerung von Systemelektronik. Rechtecksignale mit hohen Spannungsamplituden und Flankensteilheiten können die Funktion von monolithisch integrierter Niedervoltelektronik jedoch erheblich beeinträchtigen. Die Vorhersage dieser Beeinflussung vor der Fertigung solcher SoCs ist entscheidend um Gegenmaßnahmen zu treffen. Dadurch können die Gesamtfunktionalität gewährleistet und die Entwicklungskosten reduzieren werden.

Hauptziel dieser Arbeit ist es, ein geeignetes Modell zu erstellen, mit dessen Hilfe die Beeinflussung von Hochvoltpulsen auf Schaltungsblöcke mit geringen Versorgungsspannungen simulativ vorhergesagt werden kann. Die Einbettung in den üblichen Entwurfsprozess für integrierte Schaltungen ermöglicht SPICE-Simulationen ohne zusätzliche Lizenzkosten. Durch die Untersuchungen, die in dieser Arbeit vorgestellt werden, können Handlungsempfehlungen für die Integration von SoCs mit schaltenden Hochvoltspannungen und Niedervoltelektronik abgeleitet werden.

Zwei in Silicon-on-Insulator Prozessen gefertigte SoCs ermöglichen die gleichzeitige Nutzung eines Elektrolumineszenz-Elements zur Beleuchtung sowie zur kapazitiven Sensorik. Die implementierte Hochvolt-Pulsquelle kann Spannungspulse bis zu ±300 V mit Flankensteilheiten von bis zu $99.56\,\mathrm{V\mu s^{-1}}$ erzeugen. Kapazitive Lasten bis 10 nF können bei Frequenzen bis 5 kHz angesteuert werden. Parallel dazu kann ein Spread-Spectrum-Taktgeber (SST) kapazitive Sensoren mit einer Bandbreite von 10.14 MHz, einer Auflösung von 9 Bit sowie einer Dämpfung von 33.17 dB bei einer Versorgungsspannung von 5 V anregen.

Während des Schaltvorgangs der Ultra-Hochvolt-Pulsquelle kann eine Änderung der Frequenz des SST beobachtet werden. Diese lässt sich zu einem signifikanten Anteil durch die Substratkopplung erklären. Zur Verifikation des Kopplungsmechanismus werden in dieser Arbeit zum einen die relevanten Größen des Substratsnetzwerkes vermessen und mit den berechneten Werten verglichen. Zum anderen wird die Kopplung der Hochvolt-Pulsquelle auf das Substrat sowie Einflüsse von Potentialschwankungen des Substrates auf die Niedervoltelektronik messtechnisch erfasst.

Zur Vorhersage der Beeinflussung von Mixed-Signal Schaltungen kann aus dem Layout des SoCs eine Substratnetzliste extrahiert werden. Die Parameter für die Komponenten des Ersatzschaltmodells des Substrates können mit Hilfe der geometrischen Abmessungen aus dem Layout des SoCs analytisch berechnet werden. Die Substratnetzliste kann zusammen mit dem Post-Layout der implementierten Komponenten simuliert werden. Dabei ist die Modellierung der Versorgungsspannung sowie des verwendeten Gehäuses für die Simulation von großer Bedeutung. Aufgrund der gewonnen Erkenntnisse umfassen die abgeleiteten Handlungsempfehlungen für die Implementierung von SoCs mit Ultra-Hochvolt-Pulsquellen und Mixed-Signal Schaltungen neben schaltungstechnischen und layoutspezifischen Überlegungen auch Aspekte der Gehäuseauswahl. Für die gefertigten SoCs wird damit die Frequenzänderung des SST um bis zu 77,35 % reduziert.

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List of Abbreviations

3D	**Three**-**D**imensional
ASIC	**A**pplication-**S**pecific **I**ntegrated **C**ircuit
ASK	**A**mplitude **S**hift **K**eying
BCD	**B**ipolar-**C**MOS-**D**MOS
BJT	**B**ipolar **J**unction **T**ransistors
BOX	**B**urried **OX**ide
BSIM	**B**erkeley **S**hort-channel **I**GFET **M**odel
BW	**B**and**w**idth
CAD	**C**omputer **A**ided **D**esign
CM	**C**ommon **M**ode
CMOS	**C**omplementary **MOS**
D	**D**rain
DAC	**D**igital-to-**A**nalog **C**onverter
DC	**D**irect **C**urrent
DIBL	**D**rain **I**nduced **B**arrier **L**owering
DIL	**D**ual-**I**n-**L**ine
DMOS	**D**ouble-diffused **MOS**
DNL	**D**ifferential **N**on **L**inearity
DTI	**D**eep **T**rench **I**solation
DRC	**D**esign **R**ule **C**heck
DSSS	**D**irect-**S**equence **S**pread **S**pectrum
DW	**D**evice **W**afer
EDA	**E**lectronic **D**esign **A**utomation
EL	**E**lectro**l**uminescence / **E**lectro**l**uminescent
EMI	**E**lectro**m**agnetic **I**nterference
ELSE	**EL**ektrolumineszenz in kapazitiver **SE**nsorik
FET	**F**ield **E**ffect **T**ransistor
FHSS	**F**requency-**H**opping **S**pread **S**pectrum
FLS	**F**loating **L**evel **S**hifter
FSK	**F**requency **S**hift **K**eying
G	**G**ate
HiSIM	**Hi**roshima-University **S**TARC **I**GFET **M**odel
HV	**H**igh **V**oltage
HVIC	**H**igh **V**oltage **I**ntegrated **C**ircuit
HW	**H**andle **W**afer
IC	**I**ntegrated **C**ircuit
JI	**J**unction **I**solation
LDMOS	**L**ateral **DMOS**
LED	**L**ight-**E**mitting **D**iode
LFSR	**L**inear-**F**eedback **S**hift **R**egister
LS	**L**evel **S**hifter
LSB	**L**east **S**ignificant **B**it
LV	**L**ow **V**oltage
LVS	**L**ayout-**V**ersus-**S**chematic
MOS	**M**etal **O**xide **S**emiconductor

MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
MSB	**M**ost **S**ignificant **B**it
NMOS	**N**-Channel **MOS**
PDK	**P**rocess **D**esign **K**it
PMOS	**P**-Channel **MOS**
PRN	**P**seudo-**R**andom **N**umber
PSK	**P**hase **S**hift **K**eying
PSRR	**P**ower **S**upply **R**ejection **R**atio
QFN	**Q**uad-**F**lat **N**o-leads
RESURF	**Re**duced **Sur**face **F**ield
RBW	**R**esolution **B**and**w**idth
RF	**R**adio **F**requency
RMS	**R**oot **M**ean **S**quare
RTZ	**R**eturn-**T**o-**Z**ero
S	**S**ource
SOA	**S**afe **O**perating **A**rea
SoC	**S**ystem-**o**n-**C**hip
SOI	**S**ilicon-**O**n-**I**nsulator
SPIC	**S**mart **P**ower **I**ntegrated **C**ircuit
SPICE	**S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis
SR	**S**lew **R**ate
SS	**S**pread **S**pectrum
SSC	**S**pread **S**pectrum **C**lock
SSCG	**S**pread **S**pectrum **C**lock **G**enerator
TCAD	**T**echnology **C**omputer **A**ided **D**esign
TOX	**T**rench **Ox**ide
US	**U**ltra**s**ound
VBW	**V**ideo **B**and**w**idth
VDMOS	**V**ertical **DMOS**
WP	**W**orst **P**ower
WS	**W**orst **S**peed

List of Symbols

Symbol	Unit	Definition
P	W	Power
I	A	Current
C	F	Capacitance
V	V	Voltage
R	Ω	Resistance
f	Hz	Frequency
t	s	Time
Q	C	Charge
A_{BP}	-	Aspect ratio of manufacturing process
W_{D}	m	Width of depletion region
N	-	Number
g_{m}	S	Transconductance
A	m^2	Area
ϵ_{r}	-	Relative permittivity
w	m	Width of a transistor
l	m	Length of a transistor
d	m	Thickness
h	m	Height
ρ	Ωm	Resistivity
a	m^{-2}	Correction factor
b	-	Correction factor
r	Ω	Small signal resistance
Z	Ω	Impedance
D	-	Damping factor
T	K	Temperature
I_{DS}	A	Drain-source current of a MOSFET
V_{T}	V	Threshold voltage of a MOSFET
R_{th}	$\mathrm{K}\cdot\mathrm{W}^{-1}$	Thermal resistance
$A(s)$	not uniform	Transfer function
$V_{\mathrm{DS,max}}$	V	Drain-source breakdown voltage of MOSFET
$V_{\mathrm{GS,max}}$	V	Gate-source breakdown voltage of MOSFET
$V_{\mathrm{HSP,GND}}$	V	Low level voltage for driving a high-side PMOS
$V_{\mathrm{HSN,VDD}}$	V	High level voltage for driving a high-side NMOS
$V_{\mathrm{HSN,GND}}$	V	Low level voltage for driving a high-side NMOS
$V_{\mathrm{LSN,VDD}}$	V	High level voltage for driving a low-side NMOS
$V_{+\mathrm{HV}}$	V	Positive high voltage supply
$V_{-\mathrm{HV}}$	V	Negative high voltage supply
$\mathrm{clk}_{+\mathrm{HV}}$	V	Clock signal for the high-side transistor
$\mathrm{clk}_{-\mathrm{HV}}$	V	Clock signal for the low-side transistor
V_{out}	V	Output voltage of the ultra high voltage pulse generator
V_{SSCG}	V	Output voltage of the spread spectrum clock generator
f_{SSCG}	Hz	Frequency of V_{SSCG}

Symbol	Unit	Definition
V_{DD}	V	Supply voltage of the low voltage components
V_{DDH}	V	Supply voltage of buffers
V_{DDa}	V	Supply voltage for analog components
V_{DDd}	V	Supply voltage for digital components
V_{DDHV}	V	Supply voltage for clock signals of high voltage components
$V_{DD,buffer}$	V	Supply voltage for tri-state buffer

1 Introduction

1.1 Overview

Increasing the integration density of an integrated circuit (IC) has been an effort for many decades. In 1965, G. Moore first stated the trend that the number of components per integrated circuit would double every year [1]. Ten years later he revised his prediction of doubling every two years. This forecast became popular as "Moore's Law" and has become a target for research and industry.

Looking back, this trend has been followed for several decades by shrinking the size of the transistors. However, 50 years after his prediction, Moore himself is seeing an end of his forecast [2]. The actual technology node 7 nm is approaching physical limits [3].

Besides the trend of shrinking transistor sizes, the integration of microelectronic circuits in hardly any device and hence limited space for the electronic components requires that integrated circuits have implemented much more functionalities. Integrated circuits have expanded to complete system-on-chips (SoCs) as shown in Figure 1.1. Besides digital components such as processors and memories which follow Moore's Law, the integration of analog parts such as sensors and actuators, radio frequency (RF) components such as Bluetooth as well as power transistors have enabled ICs to interact with the user rather than simple computing. However, these components do not follow Moore's Law but are known as "More than Moore" [4].

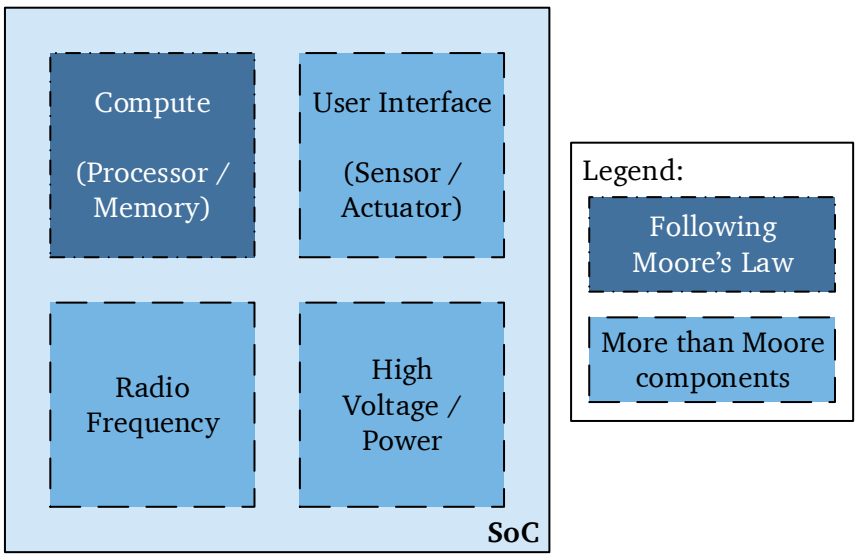


Figure 1.1.: Components of system-on-chips which follow either Moore's Law or More than Moore.

The integration density of SoCs can be further increased if several of the More than Moore components are assembled on one chip. Focusing on high voltage (HV) and power ICs, so-called Smart Power ICs (SPICs) are commonly used where different operating voltages within a single die are required [5]. They enable the monolithic integration of sensing circuitry, digital control as well as power control. A rising number of applications require the use of voltages that exceed the low voltage (LV) supply of 1.8 V, 3.3 V or 5 V. In literature, voltages of 10 V and above are already discussed as being high [6, 7, 8, 9]. However,

technologies enable the integration of power transistors which can withstand several hundreds of volts within the IC [10, 11, 12, 13] which is often also referred to as ultra high voltage. In this thesis, high voltage integrated circuits (HVICs) may be defined as ICs with devices that can withstand at least 200 V. In the following ultra high voltages may be also referred to as high voltage for the sake of readability.

High voltage ICs can reduce product costs and chip size due to the monolithic integration of power devices and signal control circuitry. Furthermore, HVICs can increase the system reliability by avoiding, inter alia, off chip connections [14]. A number of HVIC applications have been reported which are, among others, motor drive applications [11, 15], electrostatic and polymer actuators [16] as well as ac/dc power conversions [12] and electroluminescent (EL) devices [17, 18]. High voltage gate drivers are also widely used in traction systems of electrical cars and for renewable energy systems [12]. Most of these applications require alternating high voltages.

The application which underlies this thesis is a capacitive sensor which is lighted by electroluminescence. Electroluminescent devices have the great advantage that the surface lighting can be manufactured with height of only a few micrometers. To keep the space of the overall system as small as possible, it is particularly important that the electronic components for controlling the EL device and the capacitive sensor occupy as little volume as possible. Therefore, the monolithic integration of EL control and sensor excitation is the preferred solution for the overall system.

For driving the electroluminescent devices an alternating high voltage is required. H-bridge based concepts are often used for the EL excitation. However, in safety critical environments, the front electrode of the EL device is preferably ground referenced which is why an offset free single-ended switching high voltage is required at the second electrode of the EL. Therefore, a three-state ultra high voltage pulse generator has to be implemented to be able to drive the EL with a positive and a negative high voltage as well as to short the two electrodes of the EL device by setting the output of the pulse generator to ground. The capacitive sensor excitation has to be robust in harsh environments. Hence, a spread spectrum approach is chosen. The necessary spread spectrum clock generator (SSCG) has to be implemented in the low voltage domain due to electromagnetic compatibility issues. The combination of these two components on the same die requires the usage of a high voltage integrated circuit.

The integration of high voltage pulse generators and low voltage mixed-signal devices in an HVIC can cause interferences and parasitic coupling between each other. The influences on low voltage circuitry increase with the maximum amplitude of the voltages within the IC. Especially switching high voltage devices as for example for inductive or capacitive loads have a high potential to disturb other components on the chip.

Depending on the technology and output load, the switching can activate parasitic NPN transistors in conventional bulk CMOS [19] or enable capacitive coupling in silicon-on-insulator (SOI) technologies [20]. These influences can decrease the system performance or even cause failures within the LV circuitry. Therefore, it is mandatory to predict the influences at an early stage of the IC design or even minimize them by design considerations. Although the problem of high voltage interferences is already well known, it is not covered within the conventional analog or mixed-signal design flow.

1.2 Research Scope and Contribution

This thesis investigates the monolithic integration of a high voltage pulse generator along with a low voltage spread spectrum clock generator which is used for capacitive sensor excitation. A special focus is put on the required chip area, which should be kept as small as possible.

The main objective of this work is to show that high voltage components can be integrated with sensitive low voltage components without interaction on a single IC. The thesis deals with the prediction of the interferences in the design between high voltage and low voltage components and thereby addresses the high voltage low voltage co-design. As a result, recommendations can be derived as to which measures can be taken to minimize mutual interference. The following questions are answered in this thesis:

- **Is it possible to monolithically integrate and manufacture ultra high voltage pulse generators and low voltage components interacting independently?** More than Moore technologies enable the fabrication of such ICs. The influences are therefore the focus of this work.

- **How can influences between high voltage and low voltage devices be predicted in the design phase already?** The existing post-layout simulation tools are not sufficient to predict the influences. Therefore, this work deals with the question of which extensions help close this gap. The extension of the IC design flow shall be integrated in conventional computer aided design (CAD) tools for easy use by IC designers.

- **What measures can be taken to minimize the influence of switching high voltages on other circuit components such as mixed-signal devices?** It takes into account the choice of technology, the circuits design and layout considerations as well as relevant aspects of assembly and packaging issues.

1.3 Thesis Outline

The overall structure of the thesis is illustrated in Figure 1.2. After a short introduction in this chapter, high voltage technologies and devices are discussed in chapter 2. Special focus is dedicated to double diffused metal oxide semiconductor (DMOS) transistors which is the most used power transistor [21]. Different structures of DMOS devices are presented and grouped with respect to fabrication issues. Isolation techniques between high voltage and low voltage devices are discussed as they have a high impact on minimizing coupling effects.

Chapter 3 presents a system-on-chip and discusses its different building blocks. First, a sample application is presented from which specifications are derived. Different high voltage pulse generator topologies and their challenges of integration are discussed. Special focus is dedicated to the required chip area. The implemented architecture is presented. Thereafter, the capacitive sensor excitation method is explained and the different building blocks of the implemented circuitry are investigated. The chapter closes with measurement results of the fabricated SoC for the high voltage pulse generator and the mixed-signal design.

Chapter 4 discusses the coupling effects between the high voltage and the low voltage components. It focuses on substrate coupling effects within the handle wafer of silicon-on-insulator wafers. For this, a parasitic substrate model is investigated. With the help of technology computer aided design (TCAD) simulations, corrections factors, which represent fringing effects, for the calculation of the parameter values with simple formulas are presented. The substrate model enables the co-simulation of high voltage and low voltage circuitry using standard simulation programs with integrated circuit emphasis (SPICE). To finish, this chapter compares measurement results with SPICE and TCAD simulations for the parasitic substrate coupling. By applying the extracted model, the measured influences of high voltage switching to mixed-signal devices are validated by simulations.

Based on the findings of the presented studies, design recommendations for high voltage integrated circuits with mixed voltage functionalities are derived in chapter 5. It reflects on considerations during the design phase of a HVIC as well as on assembly and packaging issues.

Finally, chapter 6 summarizes and concludes the research results and gives an outlook on further research topics.

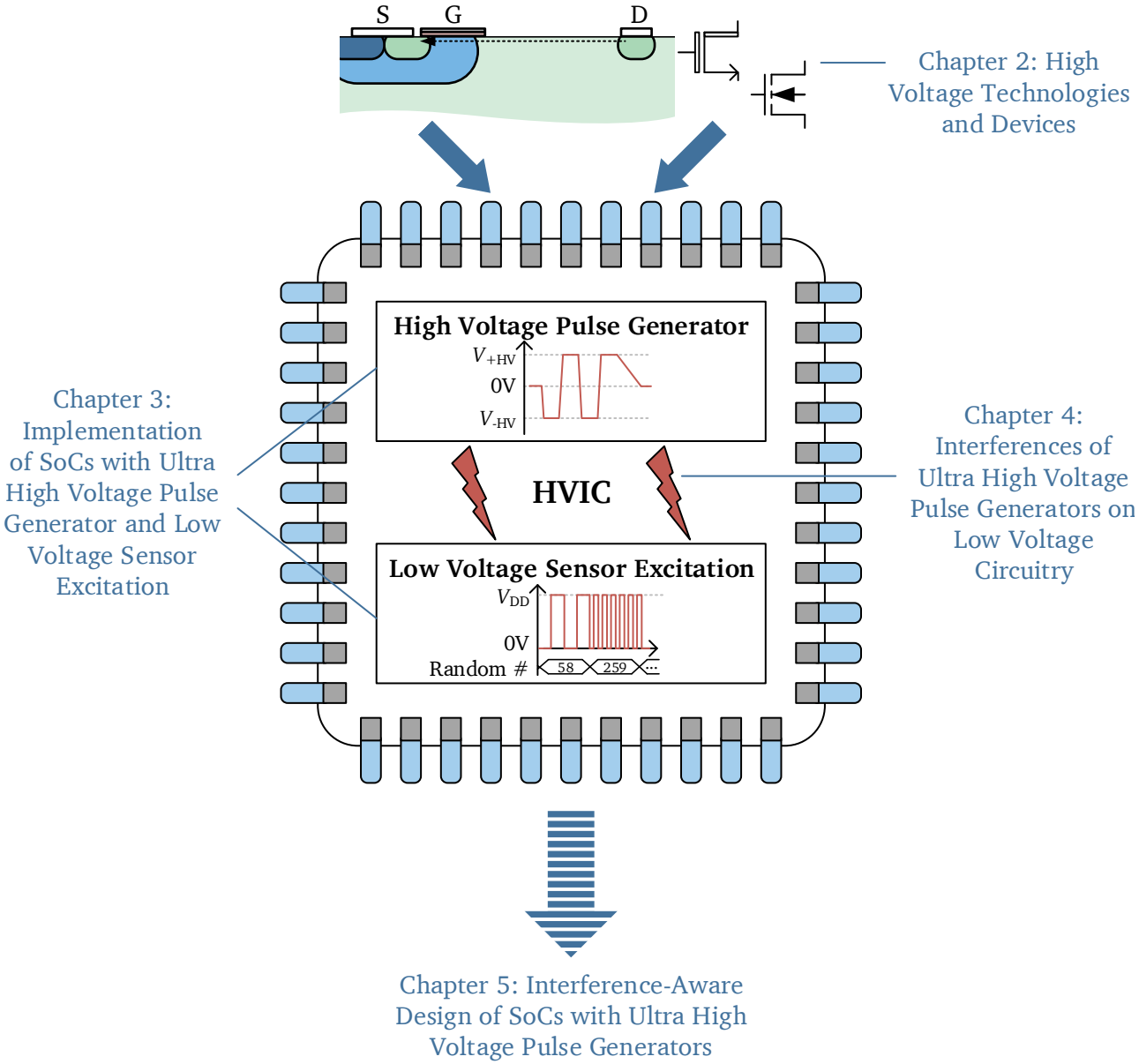


Figure 1.2.: Illustration of the thesis outline.

2 High Voltage Technologies and Devices

In order to integrate high voltage and low voltage components on an IC, existing CMOS and SOI technologies have been extended by high voltage devices. In contrast to low voltage mixed-signal devices, high voltage transistors require high breakdown voltages between drain (D) and source (S), referred to as $V_{\mathrm{DS,max}}$, and often also between gate (G) and source, referred to as $V_{\mathrm{GS,max}}$. Furthermore, low on-resistances R_{on} of the transistors are needed, since otherwise high power losses and voltage drops can be expected even at low currents [22].

The increasing interest in HVICs drives the foundries to extend their portfolio of technologies. High voltage devices are available both in conventional bulk CMOS as well as in silicon-on-insulator technologies. An overview of technologies offering transistors with drain-source breakdown voltages larger than 300 V are listed in Table 2.1.

Table 2.1.: Comparison of available high voltage technologies for drain-source breakdown voltages $V_{\mathrm{DS,max}}$ above 300 V.

Process name	Technology	Company	$V_{\mathrm{DS,max}}$ [V]	min. structure size [µm]	Data sheet
XDH10	SOI	XFab	700	1	[23]
XDM10	SOI	XFab	350	1	[24]
XU035	Bulk	XFab	700	0.35	[25]
180UHV	Bulk	GlobalFoundries	700	0.18	[26]
0.35BCD	Bulk	Nuvoton	700	0.35	[27]
0.6UHV CDMOS	Bulk	Nuvoton	700	0.6	[28]
TS100	Bulk	TowerJazz	700	1	[29]

To enable the fabrication of ICs with building blocks operating at different voltages, smart power IC technologies mostly combine three different process steps for one single IC. The combination of bipolar transistors for sensitive analog circuitry, complementary metal oxide semiconductor (CMOS) devices for efficient digital control logic and double diffused metal oxide semiconductor transistors for high voltage applications are well known as bipolar-CMOS-DMOS (BCD) technology [5].

Although investigations have been made to integrate insulated-gate bipolar transistors (IGBTs), DMOS transistors are mostly used for high voltages within high voltage ICs [21]. Output stages that generate high voltage pulses, which are the focus of this thesis, are often built with DMOS transistors which is why their structure is discussed in this chapter. In order to suppress the influences of high voltage transistors on low voltage mixed-signal designs, isolation techniques have been investigated and introduced in various technologies. The most important of these, junction isolation (JI) and dielectric isolation (DI), are presented. Thereby, the choice of technology plays a significant role, since different methods can be used depending on the basic material of the wafer. Finally, the design flow for HVICs is presented and special requirements compared to pure low voltage CMOS implementations are discussed.

2.1 Double Diffused Metal Oxide Semiconductor Transistors

The double diffused metal oxide semiconductor transistor owes its name to the manufacturing process, during which two diffusion steps are necessary. The cross section of a completely manufactured, fully

functional vertical HV DMOS transistor is shown in Figure 2.1. During the manufacturing process, the p-well as well as the n^+-regions do not go underneath the polysilicon gate area. Instead, the gate oxide and the gate polysilicon are deposited before the p-well and n^+-regions are formed. The gate oxide is subsequently used as a mask for the following diffusions. The p-well is implanted first and diffuses under the gate oxide during an annealing step at high temperatures. Hence, the channel of the DMOS is formed during this annealing step and is not dependent on any lithography mask [30, p. 346]. However, it strongly depends on process parameters such as time and temperature. Afterwards, the n^+-regions are implanted to form the source contacts. A second annealing step follows so that the doping profile expands below the gate oxide. Due to the two doping steps, the transistor is called doubled diffused MOS. Analogous to low voltage transistors, the DMOS transistors are also used as voltage-controlled current sources. Hence, the drain-source current can be controlled by the gate-source voltage.

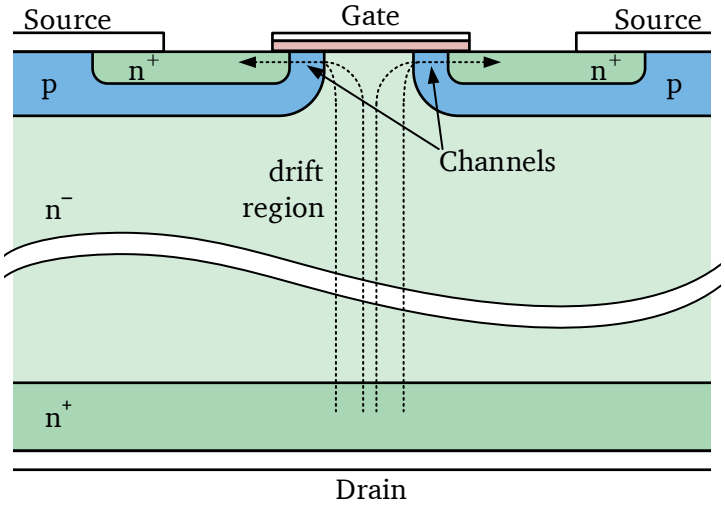


Figure 2.1.: Cross section of an n-channel vertical DMOS transistor (VDMOS) (adapted from [14]).

The breakdown voltages of the transistors are indicated by two different parameters. On the one hand, the maximum gate-source voltage $V_{GS,max}$ is important in order to not destroy the component. It is defined by the thickness and dielectric strength of the gate oxide. It is usually in the range of 5 V to maximum 20 V for HV DMOS transistors. On the other hand, voltages of several hundred of volts can be applied between drain and source. This high voltage compatibility is achieved by a voltage drop across a drift region forming a resistive path caused by a significant distance between drain and source of the transistor. An electric strength of up to 700 V can be achieved for integrated circuits (see Table 2.1).

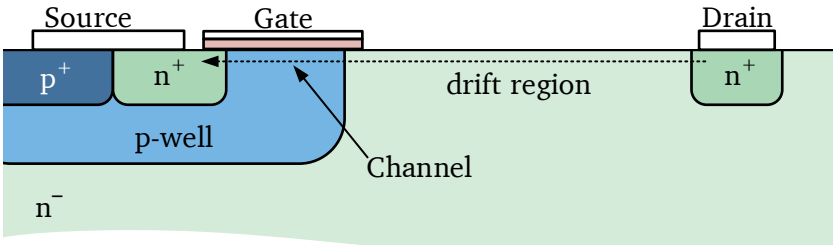


Figure 2.2.: Cross section of an n-channel lateral DMOS transistor (LDMOS) (adapted from [14]).

With regards to their structures, HV DMOS transistors can be grouped in two different types. Vertical double-diffused MOS (VDMOS) have a vertical current flow, orthogonal to the surface of the die. The drain contact is located at the bottom of the die substrate. The source contact can be at either side of the gate oxide (see Figure 2.1). The current in lateral DMOS (LDMOS) transistors flows parallel to the surface of the die. The drain contact is separated from the source by a drift region, as shown in Figure 2.2. For

LDMOS devices, reduced surface field (RESURF) techniques can be applied to reduce the on-resistance of the transistor [31]. P-channel DMOS devices can also be fabricated using the inverted doping scheme.

2.2 Isolation Techniques between High Voltage and Low Voltage Devices

Depending on the wafer material, smart power technologies offer different isolation techniques to block the high voltage influences on low voltage nodes. Junction isolation and dielectric isolation are the two main principles which are applied to counteract interferences in high voltage SoCs and hence protect the low voltage circuit from a high voltage damage [5]. Self isolation techniques, as a third method, can be used when the devices are inherently reverse-biased. However, this technique does not provide good insulation since high voltage and low voltage devices share a common terminal. This is why it is not considered. Instead, junction isolation and dielectric isolation are discussed in the following.

2.2.1 Junction Isolation

The idea of the junction isolation technique is to separate different silicon areas from each other by implementing reverse biased pn-junctions around the active areas. Figure 2.3 shows the cross section of a p-substrate wafer with junction isolation between the high voltage and the low voltage transistors. The p^+-doped junction has to be connected to the lowest potential, e.g. ground, to reverse bias the pn-junctions to adjacent n^--doped regions.

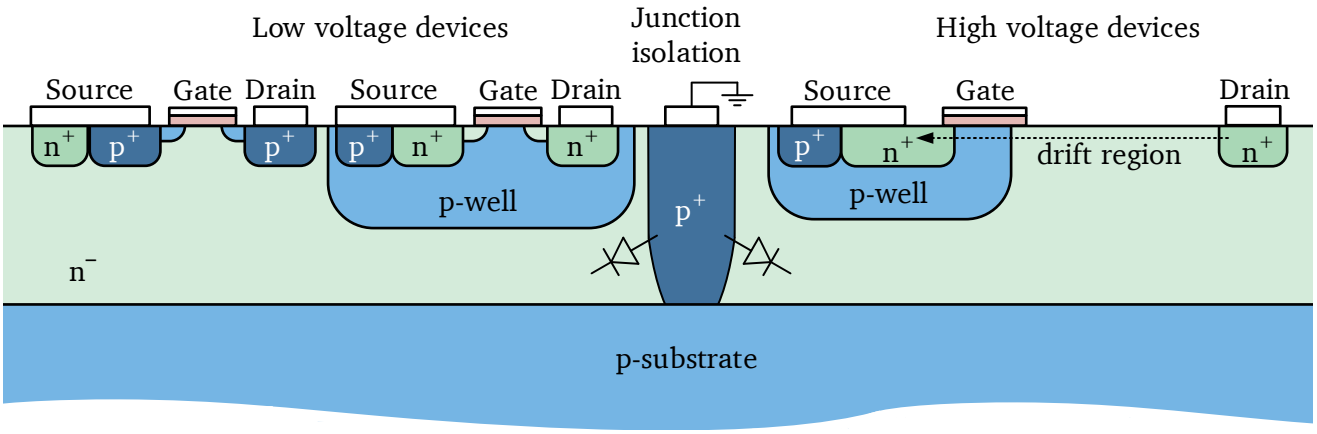


Figure 2.3.: Cross section of high voltage and low voltage transistors separated by junction isolation (adapted from [14]).

The p^+-doped junction isolation represents an additional path to ground. Coupling currents which might be introduced into the n^--doped or even p-substrate regions due to high side switching can be captured by the junction isolation [14].

2.2.2 Dielectric Isolation

Dielectric isolation is based on the separation of the two voltage domains by an insulating material. It provides better isolation compared to the above described junction isolation [12]. Furthermore, low leakage currents, high degree of integration as well as high temperature compatibility are benefits of using dielectric isolation for high voltage ICs. In addition, dielectric isolation enables completely different circuit topologies due to galvanic isolation [32].

Figure 2.4 shows the cross section of high and low voltage transistors on an n-substrate wafer separated by dielectric isolation. The isolation is achieved by narrow trenches fabricated by the Bosch process. The trenches are filled with silicon oxide at the sides and a polysilicon filler in between [33]. In addition to dielectric isolation which can be added in standard CMOS bulk processes, the substrates of the active devices can be completely separated by a horizontal dielectric layer, called buried oxide (BOX). This type of wafer is called silicon-on-insulator.

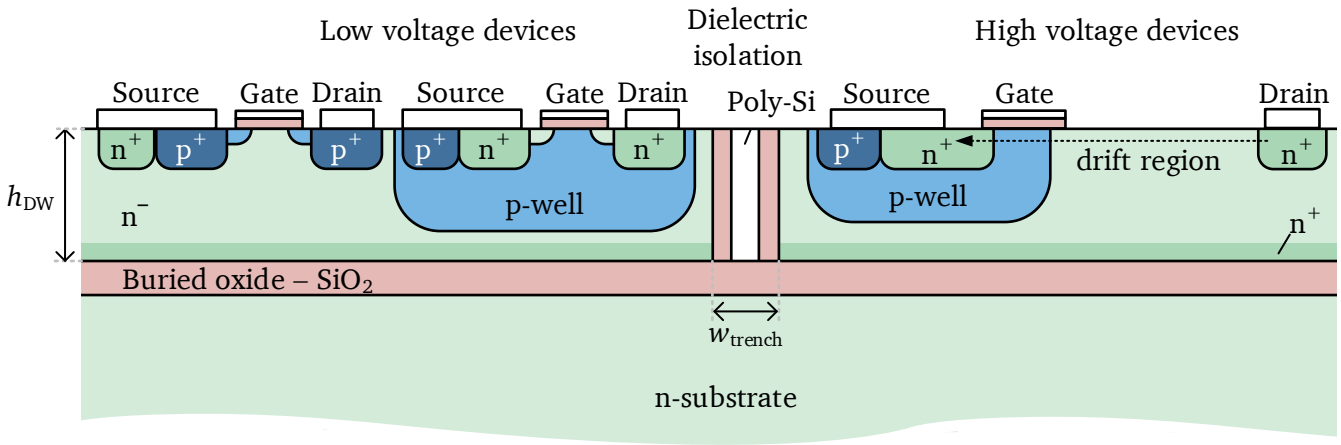


Figure 2.4.: Cross section of high voltage and low voltage transistors separated by dielectric isolation (adapted from [14]).

Although a variety of different approaches have been investigated in the past, today, dielectric isolation is mostly realized using silicon-on-insulator wafers. There are a number of manufacturing processes, which are described for example in [34]. Classically, SOI wafers with thick BOX ($\geq$2 µm) are manufactured by surface direct bonding techniques. Figure 2.5 shows the manufacturing process of SOI wafers. Two lightly n-doped wafers, the device wafer (DW) for the active circuitry and the handle wafer (HW) for stability, are oxidized up to the required thickness of the oxide. Afterwards, the two wafers are put on top of each other and bonded. As the last step, the device wafer is ground to the desired layer thickness and finally polished. This combination of stacked and bonded wafers provides the starting wafer material for SOI processes with thick BOX and thus for dielectric isolation.

The width of the trenches w_{trench} results from the device wafer height h_{DW} and the aspect ratio A_{BP} of the dielectric trenches that can be achieved with the manufacturing process

$$A_{\text{BP}} = \frac{h_{\text{DW}}}{w_{\text{trench}}}. \tag{2.1}$$

For typical device wafer heights of 55 µm [13] and aspect ratios of the Bosch process of $A_{\text{BP}} = 15:1$ [33] a minimum trench width of

$$w_{\text{trench}} \geq \frac{h_{\text{DW}}}{A_{\text{BP}}} = \frac{55\,\mu\text{m}}{15} = 3.67\,\mu\text{m} \tag{2.2}$$

can be achieved.

The use of SOI wafers as a starting material allows to integrate quasi-vertical DMOS transistors reducing the required chip area. As presented in Figure 2.1, the current flows orthogonal to the wafer surface. In SOI processes, the drain contact at the bottom of the VDMOS can be connected at the surface by the help of highly-doped vertical connections close to the dielectric isolating trenches as shown in Figure 2.6.

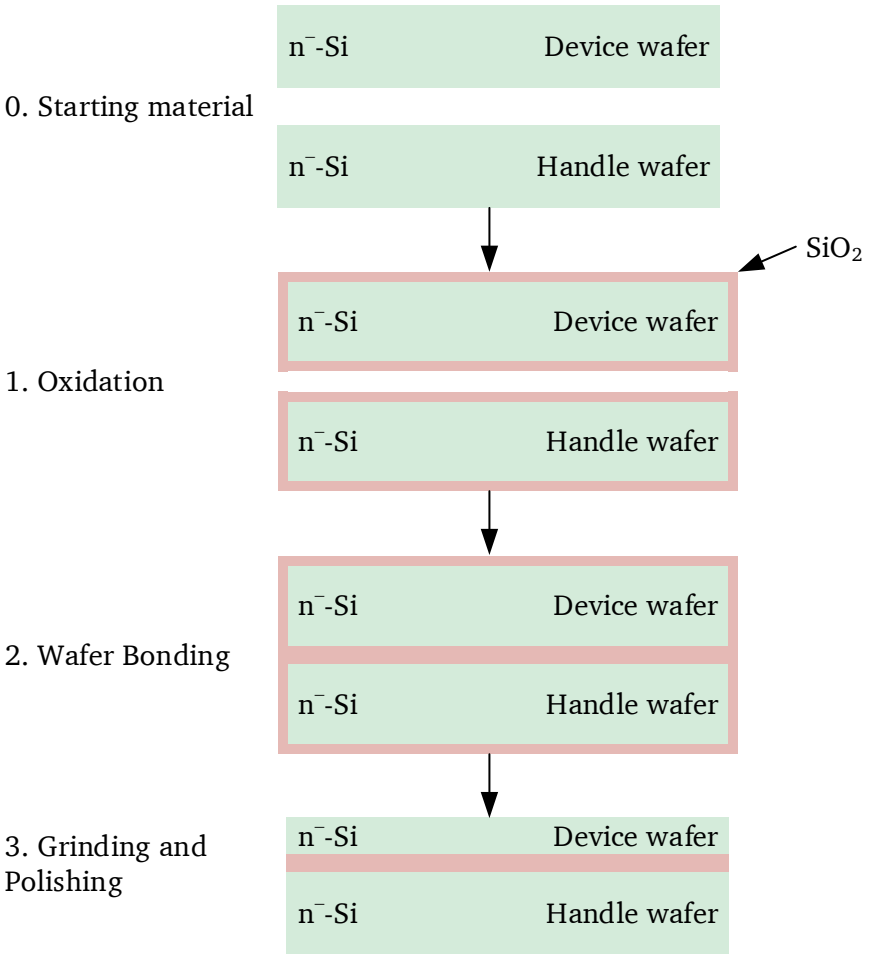


Figure 2.5.: Schematic illustration of the surface direct bonding process for manufacturing SOI wafers (adapted from [34]).

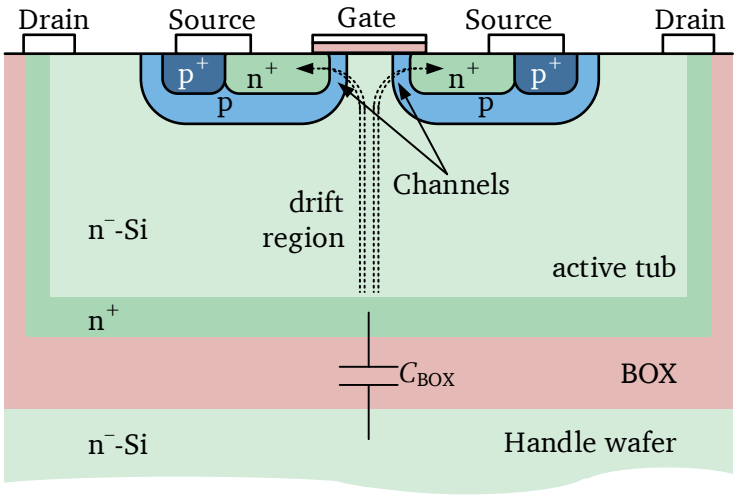


Figure 2.6.: Cross section of a quasi-vertical DMOS transistor in SOI technology (adapted from [35]).

2.2.3 Comparison of Junction Isolation and Dielectric Isolation

Benefits and drawbacks of the junction isolation as well as the dielectric isolation technique are compared in this subsection. Technical as well as non-technical aspects are discussed.

Only a few commercially available bulk technologies offer dielectric isolation [36]. Junction isolation is preferred since they require less additional process steps which reduces the production costs [36]. Due to the larger mass and simpler construction of the base material, the wafer costs for JI are lower than for DI. In contrast to this, dielectric isolation has three major advantages compared to JI. Technically, the biggest advantage is the full isolation due to the complete enclosure of active tubs by a dielectric material. This minimizes the influence of HV components on other circuitry. The resulting low leakage currents allow high operating frequencies. Therefore, monolithic integrated HV circuits which require a lot of power along with high-precision low voltage signals are preferably fabricated in a dielectric isolation process [5].

Another advantage of dielectric isolation over junction isolation is the temperature resistance. Integrated power stages can dissipate a lot of heat. In JI processes, the heat causes high leakage currents, the static power consumption increases. This can be prevented by using DI [5].

In contrast to the higher process costs of dielectric isolation over junction isolation, the chip size is reduced due to smaller transistors and shorter distances for DI processes. In general, one can say that the width of the insulation and thus the distance between HV and LV components is greater for JI than for DI. This is justified by the thickness of the depletion region W_D which occurs for JI. From physics, W_D is given by

$$W_\mathrm{D} = \sqrt{\frac{2\epsilon_0\epsilon_\mathrm{r}V_\mathrm{max}}{qN_\mathrm{D}}} \tag{2.3}$$

with ϵ_r being the permittivity of the silicon material, ϵ_0 being the vacuum permittivity of $8.85\cdot10^{-12}\,\mathrm{F{\cdot}m^{-1}}$, V_max being the maximum applied voltage within the process, q being the elementary charge of $1.602\cdot10^{-19}\,\mathrm{C}$ and N_D being the donor doping concentration of the n-region [37, p. 97]. It clearly shows that the depletion region increases with the applied voltage. Hence, for higher breakdown voltages, the junction isolation requires more chip area and the distance between the different components increases. Assuming a doping concentration of $1{\cdot}10^{15}\,\mathrm{cm^{-3}}$ [37] for lightly n-doped silicon, a permittivity of 11.7 [38] and a maximum voltage of 700 V, a junction width of 30.09 µm can be calculated by Equation 2.3 which is 8.19 times higher than the trench width w_trench for dielectric isolation calculated by Equation 2.2. Since the dielectric isolation is independent of the applied voltage, it is beneficial for higher voltages. Not only the depletion region width increases with higher breakdown voltages but also the cell size of the transistors themselves since the drift region has to be enlarged [5]. In [5], the increase of the transistor area is discussed. It is concluded that the higher production costs for DI processes are compensated by the smaller chip area for voltages above 100 V [5, p. 109]. Hence, dielectric isolation techniques and SOI processes become more economical as the breakdown voltage of the devices increases.

2.3 Design Flow for High Voltage Integrated Circuits

Compared to pure low voltage CMOS IC design, the development process of high voltage SoCs require the consideration of HV specific issues. While implementation of functionality plays the most significant role in low voltage ICs, HVICs must take into account the peculiarities of high voltage components on the chip. On the one hand, these are given by the high voltage per se and on the other hand by the large chip area of the HV transistors [22].

High voltage ICs have been historically introduced in conventional CMOS processes with minimum feature sizes of 0.5 µm or larger [10], the majority of the chip area is mostly occupied by analog components. This is why the design flow for HVICs follows the analog ASIC design flow, shown in Figure 2.7.

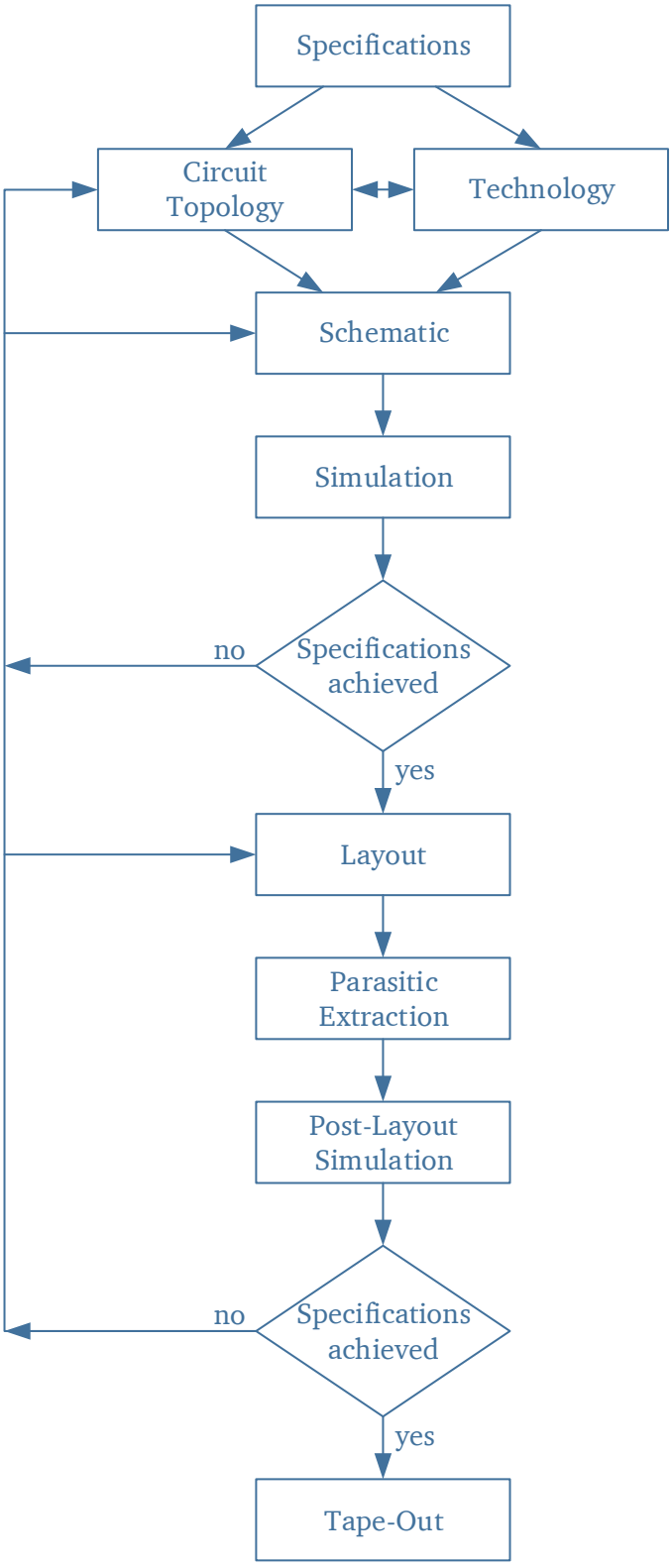


Figure 2.7.: Design flow for high voltage integrated circuit following an analog implementation.

Based on the given specifications for a particular application, a technology can be chosen which fulfills not only the breakdown voltage specifications and electrical properties such as on-resistances but also lifetime and cost requirements. Besides, circuit topologies can be derived from the specifications. For the high voltage building blocks, the variety of available circuit topologies is limited. Therefore, the designer often has to modify existing low voltage topologies. The promising approach can be implemented in a schematic entry using the primitive devices of the technology such as transistors, resistors, capacitors and diodes. These are given by the foundry in the so called process design kit (PDK). If it turns out that the circuit is not feasible in the chosen technology, either the technology or the circuit must be adapted.

If the implementation of the desired circuit in the selected technology is possible, the transistor level implementation can be simulated. SPICE models are given within the PDK. Whereas low voltage transistors are mostly modeled by the Berkeley Short-channel IGFET Model (BSIM) [39], high voltage DMOS transistors are modeled by the Hiroshima-University STARC IGFET Model (*HiSIM*) [40]. These models are surface-potential based models which solve the Poisson equation [41]. For power devices with several hundreds volts, the low voltage model has been extended by a drift region resistance to *HiSIM-HV*. The model includes specific effects caused by the drift region such as resistive drop, capacitances and self-heating due to the power losses [42]. The HiSIM-HV model is the industry standard for high voltage and power devices since 2009 [43]. Although the model has been developed for LDMOS devices, it mainly shows good conformity for quasi-vertical DMOS transistors [44].

A variety of simulations can be performed to ensure the functionality of the IC before manufacturing. These include not only DC, AC and transient simulations but also temperature, noise, corner and process mismatch simulations. For the design of HVICs, specific issues have to be addressed such as safe operating area (SOA) checks. SOA checks have to be performed for every possible operating condition to exclude breakdowns under all circumstances and to ensure sufficient life time of the devices. Typically, all of these simulations can be performed with one electronic design automation (EDA) tool such as Cadence® Virtuoso® and Spectre®. In general, simulations with high voltages can cause convergence problems because the simulators are optimized for the low voltage domain. In addition, electro-thermal co-simulations may be important in the design phase of HVICs, as the high voltage can cause significant power dissipation in the chip even at low currents.

When the simulation results meet all specifications, the layout of the circuit can be made. Otherwise, the circuit implementation has to be adjusted until all requirements are met. The layout of the high voltage standard devices is predefined by the foundry. When assembling the standard components, sufficient guard rings, junction isolation or trenches have to be considered to minimize coupling effects to adjacent components. Since high current peaks can occur in high voltage switching devices, it is advisable to increase the width of the metal signal routing which also reduces voltage drops across the routing layers. Design rules as for example for minimum widths and distances within certain layers are technology-specific and given by the foundry in the PDK. Compliance with these rules can be checked with the so-called design rule check (DRC). The EDA tools help to detect any discrepancies between the electrical signal connection in the layout and the schematic entry by layout-versus-schematic (LVS) tests.

If DRC and LVS tests are passed successfully, parasitic elements such as resistances of wires and interconnects as well as capacitances between layers within the layout can be extracted by parasitic extraction tools such as Cadence® Assura®. Inductance and substrate network extraction are not always supported by the PDK. System degradation or even failures of the integrated circuits might be predicted by post-layout simulations. Again, the whole range of simulations can be performed. Due to the high number of parasitic components, the feasibility of these simulations is limited by the available computing power and available time.

If the specifications are met by the post-layout simulations, the design can be sent to the foundry for fabrication. Otherwise, improvements or necessary rectifications can be carried out throughout the complete design flow which directly influences the design cost of the ASIC. After successful implementation, the layout data can be sent to the foundry for production (Tape-Out).

After manufacturing, the implemented functions of the IC can be validated by measurements. Conclusions on the process corner and the interactive influence of the various components on the chip can be drawn. Despite intensive simulations and the consideration of HV specific requirements, failures are still comparatively high in HVICs due to parasitic impacts of the high voltage [45]. Although special physics-based tools such as technology computer aided design software could help to predict these influences, this approach is not often used due to several reasons. In part, this is due to the fact that accurate descriptions of the material parameters within the technology such as doping profile are needed for the TCAD simulation. Often this information is not provided by the foundry. Assumptions and simplifications have to be made so that the accuracy and thus the usability of the simulation results is often uncertain. On the other hand, these field simulations are highly time-consuming and new software with high license costs are required. Design engineers prefer SPICE-based simulations since they are more familiar with these simulations and they are much faster. However, such an approach does not yet exist in commercial IC design tools [45].

3 Implementation of SoCs with Ultra High Voltage Pulse Generator and Low Voltage Sensor Excitation

After discussing the technologies, devices and isolation techniques of HVICs in chapter 2, an example application is explained in this chapter. The implemented SoCs include low voltage mixed-signal devices and an ultra high voltage pulse generator, which may cause possible interference. A particular focus of the implementation is on the required chip area, which is generally very large for HV components and is supposed to be minimized for the implementation within this thesis. Within the description of the example, the load is specified and possible implementations for high and low voltage circuitry will be discussed. The implemented SoCs are presented and characterized by measurements. Parts of this chapter have already been published in [46], [47], [48] and [49].

3.1 Sample Application and Specifications

In 1936, George Destriau discovered that light can be generated from Zinc Sulfide (ZnS) particles in case an electrical field is present across them [50]. Two different physical effects can be distinguished. Electron-hole pair recombination is utilized in light-emitting diodes (LEDs) whereas electroluminescent devices generate light by impact excitation of a light-emitting center, the luminescent layer [50, p. 1]. This second type of light generation requires alternating high electrical fields since the light is emitted only for a certain time after the field has been changed.

The structure of electroluminescent devices is shown in Figure 3.1. An insulation layer is deposited onto a reflecting rear electrode first. This layer protects the device from short circuits which are likely to occur due to applied high electrical fields for any imperfection of the luminescent layer [51]. The luminescent layer is printed onto the insulation layer and covered with a transparent front electrode so that light can be emitted during the operation of the devices. Finally, an encapsulation layer is deposited to protect the device from damage.

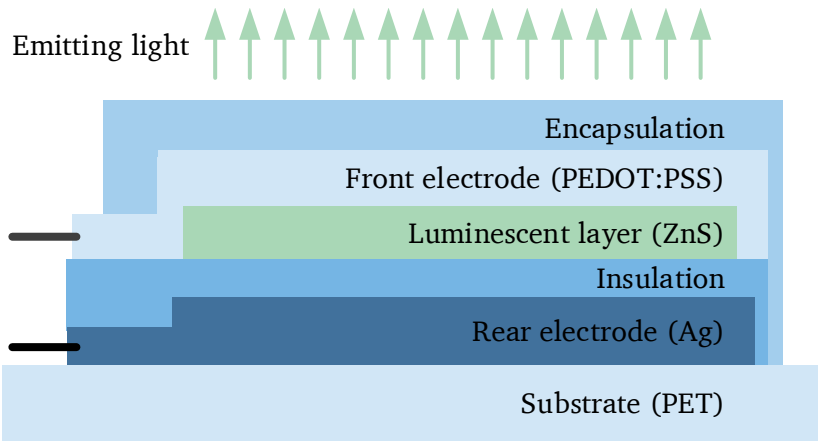
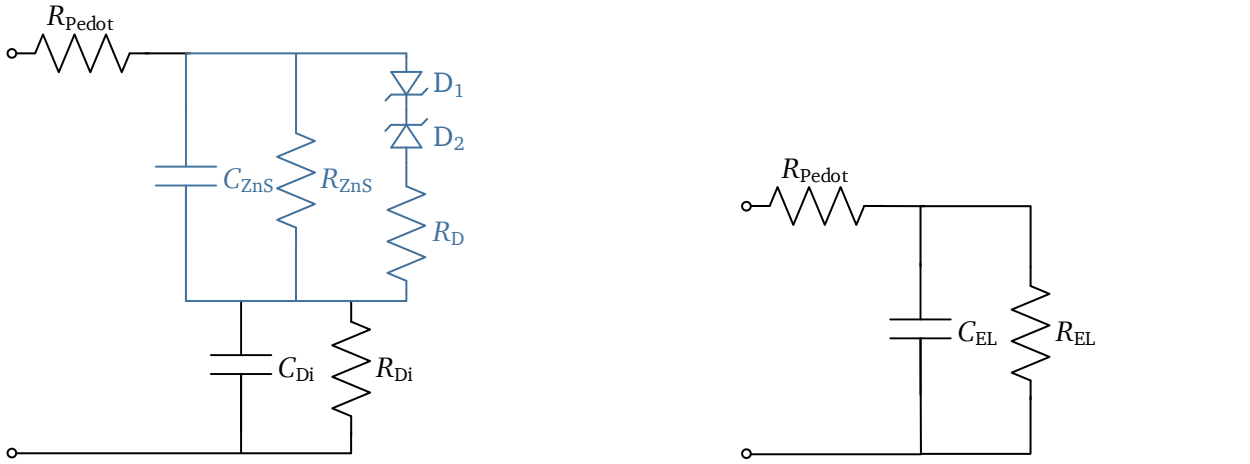


Figure 3.1.: Layer structure of an electroluminescent device.

Due to the two electrodes enclosing an insulation as well as a luminescent layer, the EL device can be electrically regarded as a lossy parallel-plate capacitor. Figure 3.2a shows a complex electrical equivalent circuit model which takes account of the electric features related to the different printed layers. R_{Pedot} is the resistance related to the transparent front electrode. C_{Di} and R_{Di} are properties related to the insulation layer. Nonlinearities can be assigned to the ZnS luminescent layer (C_{ZnS} and R_{ZnS}). Diodes D_1 and D_2 represent the threshold voltage which is required for the light emission. The latter is electrically represented as resistor R_{D}. In lighted condition, the luminescent layer can be regarded as a conductor [51]. For the design of the excitation electronics such as a high voltage pulse generator, a simple equivalent circuit for on-conditions, shown in Figure 3.2b, is sufficient [51].



(a) Complex equivalent circuit (adapted from [52]). Components assigned to the luminescent layer are shown in blue.

(b) Simplified equivalent circuit for the design of the driving electronics.

Figure 3.2.: Equivalent circuit of electroluminescent devices.

For the emission of light, an alternating high voltage above a threshold voltage is required. This threshold voltage is defined by the material and geometry. The luminance depends on the electrical excitation parameters such as amplitude, waveform and frequency [51]. In general it can be said that the luminance increases with higher amplitudes and higher frequencies. Since square wave signals contain high frequency components, the luminance is higher than for their frequency equivalent sinusoidal waveform. However, the lifetime is reduced with higher amplitudes and higher frequencies. The tradeoff between luminance, lifetime and circuit complexity has to be addressed during the design phase. Voltages of up to $600\,\mathrm{V_{pp}}$ are required within this work. To reduce circuit complexity and minimize chip size of the IC an alternating square wave output signal is aimed.

The EL technology has recently captured interest again since it can be combined with, inter alia, touch sensing functionality [53, 54, 17]. One example is presented in the ELSE-Project which aimed at lighting the symbol of a touch sensor used in buses or trams [55]. ELSE stands for the German *Elektrolumineszenz in kapazitiver Sensorik* which can be translated to *Electroluminescence in capacitive sensors*. As shown in Figure 3.3, the capacitive touch sensor is equipped with a symbol lighted by electroluminescence. This lighting technology is chosen due to its robustness and small height.

The touch functionality in combination with the EL lighting can be achieved using three different approaches as shown in Figure 3.4. The EL itself is a capacitor whose value is a function of the distance between the two electrodes. The first approach, shown in Figure 3.4a and described in [53], changes its thickness which results in a detectable capacitance change in case of pressure on the EL device. For the second approach shown in Figure 3.4b, an additional capacitor is implemented underneath the EL

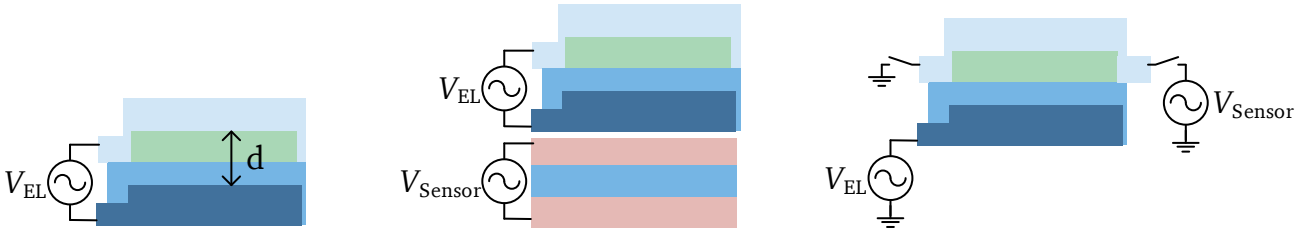
(a) Original touch sensor.

(b) Touch sensor with lighted symbol.

(c) Activated touch sensor with lighted symbol.

Figure 3.3.: Functioning demonstrator of the ELSE-project with time multiplexed EL lighted symbol and capacitive sensor.

device whose capacitance changes in case of a touch event [54]. Third, the front electrode is shared for lighting the EL and for sensor functionality as shown in Figure 3.4c. The two functionalities alternate temporally [17]. The third approach was proposed within the ELSE project. The first approach is not feasible since the thickness of the printed EL is only a few micrometer and high pressure have been expected to obtain a detectable touch event. The second approach was not applicable due to limited space of the system which is why the third approach was regarded most promising for the project.



(a) Design in [53].

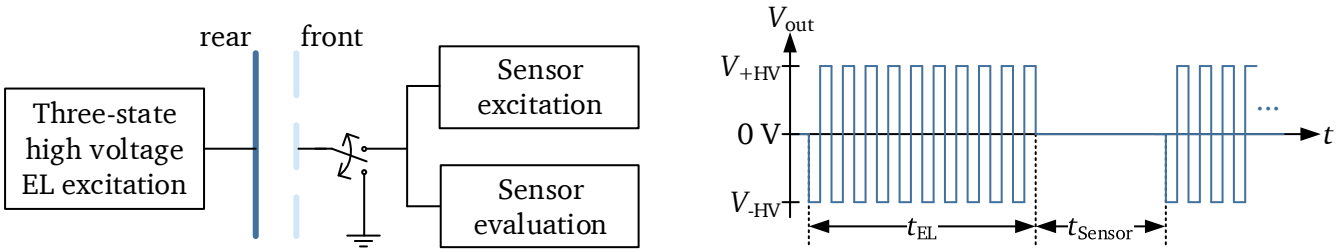
(b) Design in [54].

(c) Design in [17].

Figure 3.4.: Different approaches for the combination of EL and sensing functionality.

Due to the combination of electroluminescence with a necessity for a touchable device, special safety issues have to be considered. To protect the user from electrical shocks, the front electrode of the EL device has to be connected to ground, in addition to the printed encapsulation layer. In this way, the user is shielded from the high voltage which is required to emit light by the EL device. However, the specification within the project requires the alternating voltage of positive and negative high voltages to be connected to the rear electrode to get a DC offset free output voltage.

Figure 3.5a shows the block diagram of the overall system including EL excitation as well as sensor excitation and the sensor readout to detect a touch event. A so-called *time multiplexing* for the lighting and the sensing readout was chosen so that the two systems are not operating at the same time. When the EL is lighted, the sensor is disconnected and the front electrode is connected to ground. If the sensor is activated, the front electrode is released from ground and the EL voltage V_{out} is zero as shown in Figure 3.5b.



(a) Block diagram of the application.

(b) Proposed time multiplexing for the SoC with high voltage pulse generator and sensor excitation.

Figure 3.5.: Proposed block diagram and time multiplexing of the sample application.

The parameters for the time multiplexing, as shown in Figure 3.5b, have to be chosen in a way that the user realizes neither flickering of the light nor a delay in the touch detection. It is suggested that the EL emits light for 2 ms. During this time, frequencies of up to 5 kHz are required to emit enough amount of light. The positive high supply voltage V_{+HV} has to be up to +300 V. The negative high supply voltage V_{-HV} has to be equal in value and therefore being up to -300 V. The EL device represents a load of up to 10 nF with a parallel resistor of 10 MΩ. The transparent electrode adds a series resistance of more than 100 Ω. Table 3.1 summarizes the specifications for the high voltage pulse generator which drives the electroluminescent devices. The implementation of the high voltage pulse generator will be discussed in subsection 3.2.2.

Table 3.1.: Specifications for the implementation of the high voltage pulse generator to excite pad-printed EL devices.

Parameter	Min	Typ	Max	Unit
V_{in}		5		V
V_{+HV}	0	+300		V
V_{-HV}	-300	0		V
C_{EL}			10	nF
R_{PEDOT}	100			Ω
R_{EL}	10			MΩ
f_{out}	400		5000	Hz
t_{EL}		2		ms

The capacitive sensor has to withstand demanding environmental conditions with electromagnetic interferences (EMI). Therefore, the sensor has to be excited by a spread spectrum clock generator [56]. The project requires driving the sensor with a frequency hopping pattern. The lower frequency shall never be lower than 125 kHz due to EMI specifications. A bandwidth Δf_{SSCG} of more than 4 MHz is required for a spreading of 512 different frequencies. The capacitive sensor represents a load of 30 pF. The specifications of the sensor excitation are summarized in Table 3.2. The sensor excitation will be discussed in more detail in section 3.3.

Table 3.2.: Specifications for the spread spectrum clock generator which is used for the capacitive sensor excitation.

Parameter	Min	Typ	Max	Unit
V_{in}		5		V
$f_{\text{SSCG,min}}$	125			kHz
Δf_{SSCG}	4			MHz
Resolution		9		bit
C_{out}		30		pF
t_{sensor}		8		ms

The overall block diagram of the electronic system is given in Figure 3.6. The high voltage pulse generator for the EL excitation as well as the spread spectrum clock generator and a buffer to drive the required load is implemented within a single IC. Voltage generation and stabilization, logic control of the timing and the sensor evaluation are implemented off-chip. The two building blocks for the EL excitation and the sensor excitation are discussed in the following sections.

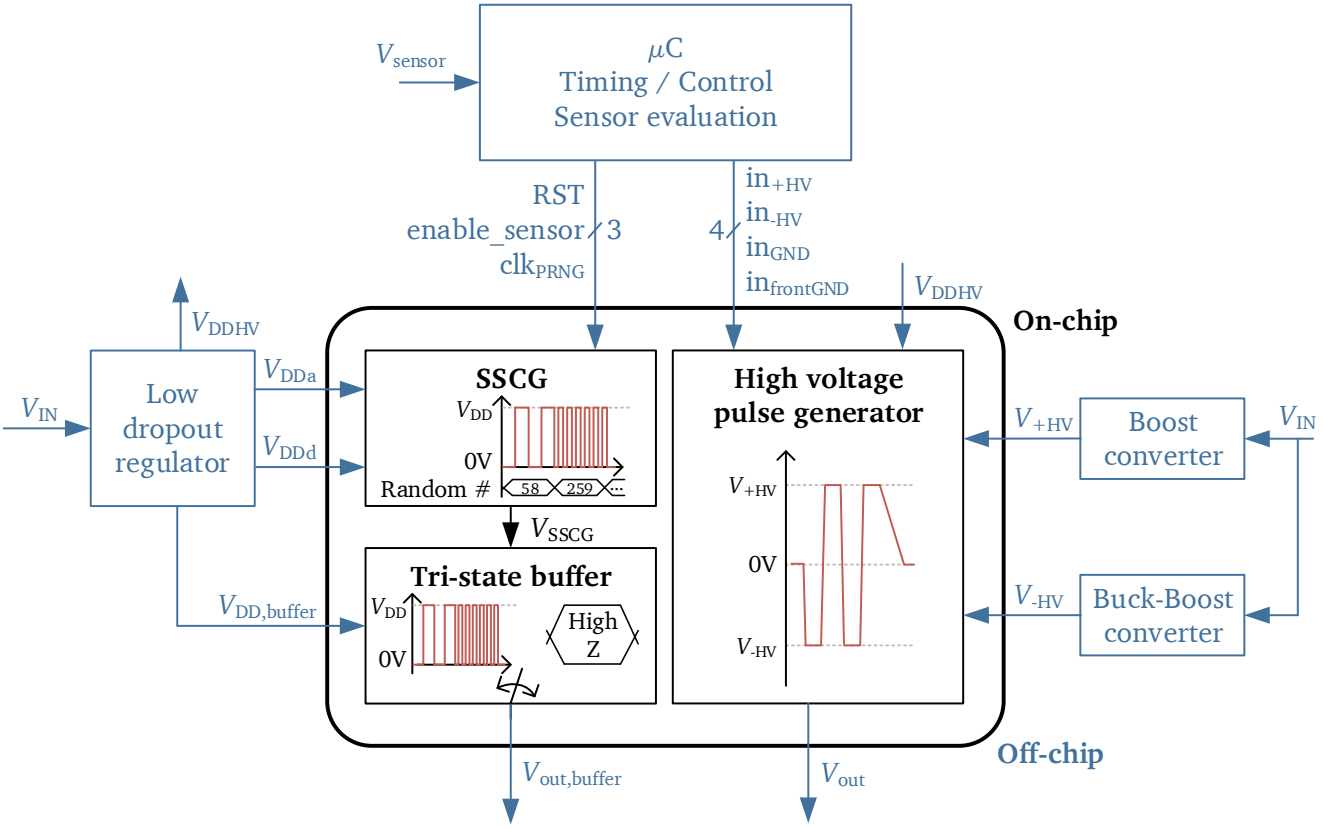


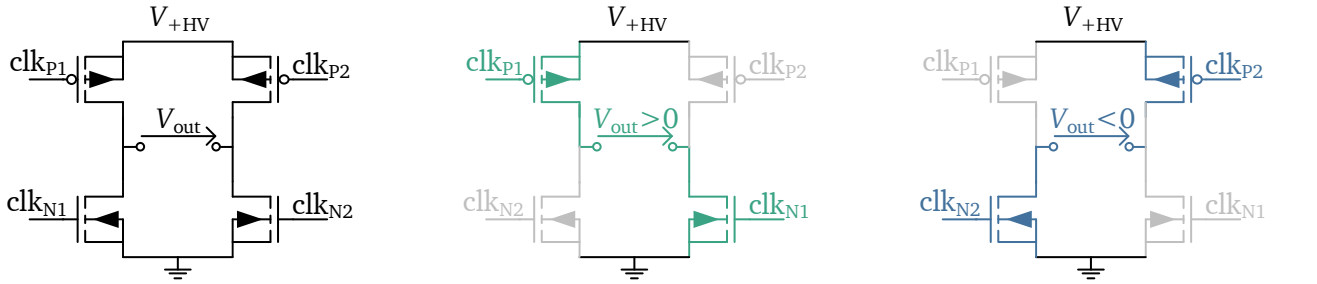
Figure 3.6.: Block diagram of the SoC with three-state pulse generator and spread spectrum clock generator as well as external components.

3.2 Three-state Fully Integrated Ultra High Voltage Pulse Generator Design

Building blocks that can transform direct current (DC) to alternating current (AC) are called inverters. They are widely used in photovoltaic systems [57, 58], inductive heating [59, 60] as well as for electric vehicles [61, 62]. Depending on the output slew rate, an inverter can also deliver output pulses as required in this thesis. The wide range of applications require inverters for different voltage and current levels. In this thesis, the term inverter may also be used as for an ultra high voltage pulse generator.

In this work, special focus is put on functional pad-printed electroluminescent devices, as presented in [63], which require an ultra high voltage pulse of up to 600 V_{pp} and high slew rates to emit light. A wide range of electroluminescent drivers are commercially available (see Table A.1 in Appendix A). However, none of these fulfill the specifications of the pad-printed devices, as shown in Table 3.1. The maximum output voltage of the commercially available drivers is 400 V_{pp} for the HV816 and the HV809 from Mircochip [64, 65]. The maximum EL driving frequency is 1500 Hz for the HV830 and the MIC4833 [66, 67]. The DC to AC conversion for all available EL driver ICs is based on an H-bridge design.

The basic schematic and the operation principle of an H-bridge is shown in Figure 3.7. The operation principle for the schematic implementation in Figure 3.7a consists of four phases of which two are discussed in more detail. In phase one, shown in Figure 3.7b, transistors P1 and N1 are operated in on-state. The voltage across the output terminals is positive. In phase two, all transistors are switched off which results in a high impedance state of the output. This phase prevents short circuit currents from the high voltage node to ground. In the third phase, shown in Figure 3.7c, transistors P2 and N2 are operated in on-state. The high voltage is connected to the opposite terminals from phase one, the output voltage is negative across the terminals in opposite direction. In this way, DC voltages can easily be converted to AC with high slew rates. The output waveform is a square wave with a differential output which is suitable for many applications.



(a) Schematic of an H-bridge.

(b) Phase 1: Output voltage is positive.

(c) Phase 3: Output voltage is negative.

Figure 3.7.: Schematic of an H-bridge output stage during operation.

As described in section 3.1, due to safety issues, the excitation voltage for an EL devices with a capacitive sensor has to be provided on a single-ended output with the ability to have a positive and a negative high voltage as well as ground. A square shaped output waveform with high output slew rate is satisfactory for the application. Since all available EL driver ICs are based on an H-bridge concept, neither they themselves nor their schematic implementation can be used for the purpose within this work.

Instead, a high voltage three-state inverter is required. It has to be able to pass positive and negative high voltages to the output as well as setting the output to ground. Although this approach will add complexity to the circuitry, it is beneficial in terms of expandability. If N elements have to be driven, an

H-bridge approach requires $2 \cdot N$ electrical connections to the devices. Compared to that, a three-state inverter requires only $N+1$ connections and is therefore more suitable for the expandibility to array applications. The following subsection describes different architectures for high voltage integrated inverters and discusses their feasibility for the depicted application. Subsequently, the implemented inverter is presented in subsection 3.2.2.

3.2.1 High Voltage Inverter Concepts

As discussed in chapter 2, integrated high voltage devices can withstand a high voltage due to a drift region between drain and source. Hence, the withstanding distance only exists for the drain-source voltage. Due to the limited thickness of the gate oxide, the breakdown voltage of the gate to source voltage is significantly lower than the drain-source voltage. To be able to drive the high voltage devices, level shifters (LS) are required to translate the low voltage level control signals into the high voltage levels V_{GHigh} and V_{GLow} within the gate-source specifications of the devices. Figure 3.8 shows the block diagram of a typical high voltage integrated circuit. The control signals are driven within the low voltage domain between ground and V_{DD}. Level shifters, also known as gate drivers, translate these signals into the high voltage domain, typically between ground and $V_{+\mathrm{HV}}$. The architecture of the gate driver is dependent on the output stage which can be implemented with a low-side NMOS and a high-side PMOS, referred to as CMOS output stage, or with high-side and low-side NMOS transistors, referred to as dual-NMOS output stage [68].

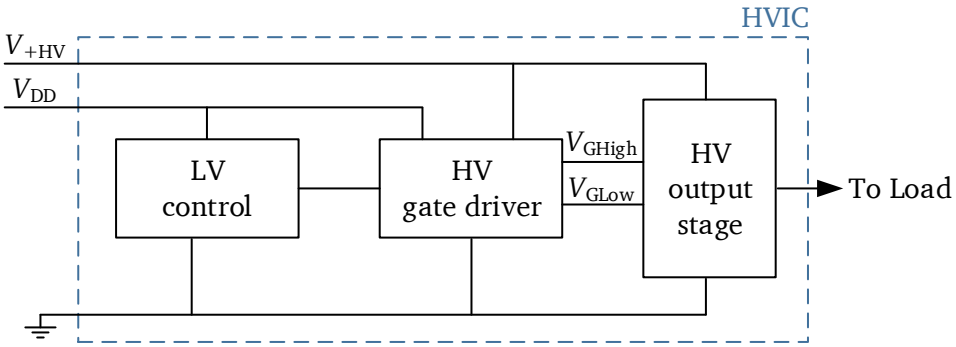
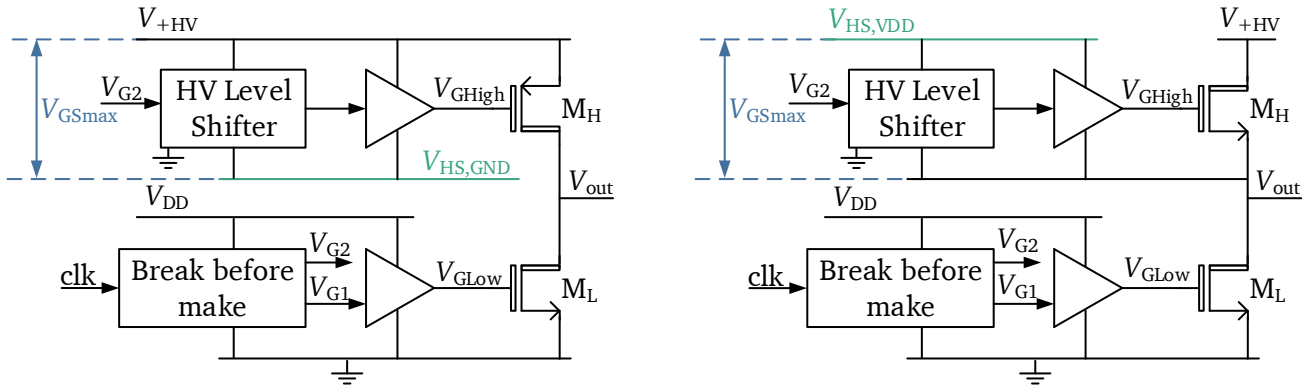


Figure 3.8.: Block diagram of a typical high voltage integrated circuit with low voltage control, gate driver and output stage (adapted from [68]).

Figure 3.9 shows two block diagrams for different high voltage output stages. The low-side driving signal V_{GLow} is ground referenced and therefore easy to implement. In contrast, the clock signal V_{G2} for the high-side transistor $\mathrm{M_H}$ has to be shifted to the high-side gate signal V_{GHigh}. This ensures that the transistor can be switched off and on without exceeding the maximal gate-source voltage of the high-side transistor $\mathrm{M_H}$. If this transistor is implemented as a PMOS transistor, the source is connected to the high input voltage $V_{+\mathrm{HV}}$ which represents the maximum supply voltage of the drive circuitry. The minimum supply voltage for the high-side transistor $V_{\mathrm{HS,GND}}$, as shown in Figure 3.9a, is a DC voltage supply and can be generated from the high voltage supply $V_{+\mathrm{HV}}$. It is maximum V_{GSmax} smaller than $V_{+\mathrm{HV}}$. For dual NMOS transistor output stages, as shown in Figure 3.9b, the output voltage V_{out} represents the floating high-side ground. The supply voltage $V_{\mathrm{HS,VDD}}$ of the driving circuitry for the high-side NMOS has to be generated being V_{GSmax} higher than the switching output voltage V_{out}. Hence, a floating power supply for the high-side driver has to be implemented.



(a) Block diagram of a gate driver for CMOS output stage.

(b) Block diagram of a gate driver for dual NMOS output stage.

Figure 3.9.: Different architectures for high voltage output stages (adapted from [68]).

Compared to HVICs with only a positive high voltage power supply, output stages with a positive and a negative high voltage, V_{+HV} and V_{-HV}, require two gate drivers, for the high-side and low-side transistor, respectively. A block diagram is shown in Figure 3.10. In literature, only a few examples of output stages with positive and negative output voltages are reported. The basic principles of these gate drivers and output stages will be discussed in the following. Wherever possible, applicable architectures and principles from single high voltage supply circuits will be cross-referenced.

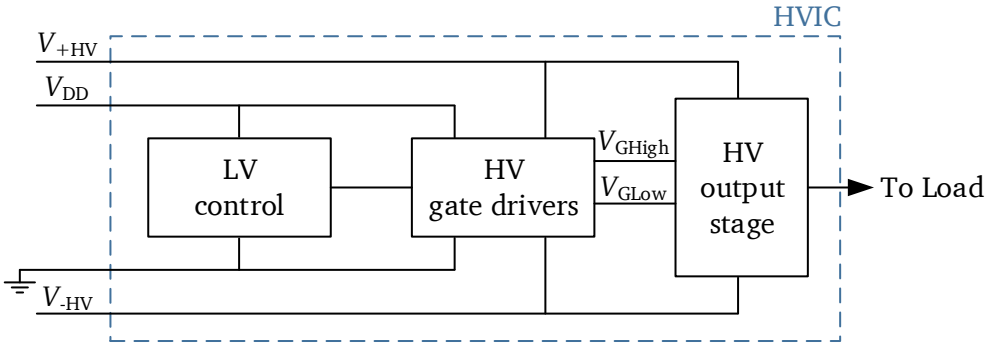


Figure 3.10.: Block diagram of a typical high voltage integrated circuit for positive and negative high voltages.

3.2.1.1 AC Coupling Level Shifter

The basic principle of AC coupled output stages is shown in Figure 3.11. The clock signals clk_{+HV} and clk_{-HV} are non-overlapping clock signals preventing short circuits in the output stage consisting of DM1 and DM2, respectively. The two low voltage clock signals are buffered to drive a capacitor each. These capacitors are connected to the gate of the high-side and low-side transistors, respectively. Charge can be transferred by the coupling capacitor to the gate of the high and low-side transistors, respectively. The gate oxide is protected from breakdown by a Zener diode between the gate and the source of each output transistor. Charge can be removed from the gate by a resistor which is connected to the positive and the negative high voltage supply.

The supply voltage of the buffer V_{DDH} can either be equal to the low supply voltage V_{DD} of the logic signals (e.g. $\mathrm{clk}_{+\mathrm{HV}}$) or the maximum gate-source voltage of the output transistor DM2 (e.g. up to 15 V). Higher amplitudes of the low-side signals result in a higher gate-source voltage at the output stage. Since the drain-source current increases with the gate-source voltage, the size of the transistor can be reduced to maintain the output current compared to low gate-source voltages.

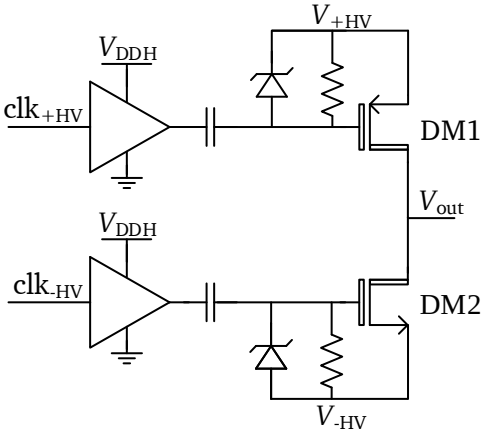


Figure 3.11.: AC coupled inverter with a high-side PMOS and a low-side NMOS transistor. The return-to-zero circuit is not shown.

An advantage of this topology is the electrical isolation of the low voltage signals from the high voltages by the coupling capacitors. Furthermore, no extra supply voltages for the low and high level signal of the high-side PMOS and low-side NMOS are required. In steady state, the power consumption of this topology is minimal since only leakage currents are parasitically flowing. Examples for commercially available AC coupled three-state inverters are the HV7360 and the HV7361 from Microchip Technology Inc.[69]. They can withstand voltages of up to ±100 V at frequencies up to 35 MHz.

The coupling capacitors require a high capacitance to deliver the charge which is required to drive the gate capacitances of the output transistors. Since the voltage difference between the high voltage and the low voltage drops across the coupling capacitor, it must be able to withstand the full high voltage. The integrated high voltage capacitors tend to have a low sheet capacitance which is why a high area consumption for the integration of the coupling capacitor is expected. The fact that this topology can only be implemented with high-side PMOS transistors also contributes to the high area expectation for this topology.

The size of the coupling capacitors can be reduced if only a small load has to be charged on the high-side instead of capacitively charging the gate-source capacitance of the output transistor. The charge can be delivered by low voltage buffers or inverters that are connected between the high voltage $V_{+\mathrm{HV}}$ and a floating ground voltage $V_{\mathrm{HSP,GND}}$ for the high-side PMOS transistor as shown in Figure 3.12. For the low-side NMOS transistor, a supply voltage $V_{\mathrm{LSN,VDD}}$ for the low voltage buffers or inverters has to be generated. If required, the number of inverters and buffers can be adapted to reduce either chip area or propagation delay. To protect the input of the first buffer, protective diodes to $V_{+\mathrm{HV}}$ and $V_{\mathrm{HSP,GND}}$ as well as to $V_{-\mathrm{HV}}$ and $V_{\mathrm{LSN,VDD}}$ are required.

Although the size of the coupling capacitors is reduced, they still have to withstand the high voltage drop and the high-side output transistor can only be implemented with a PMOS transistor. The reduction of the chip area for the capacitances have to be opposed to the area required for the implementation of the additional components. Both, the generation of the reference level for the high voltage logic and the buffer for driving the gates of the output transistors, have to be taken into account. When using

this topology, depending on the technology and the required specifications, the two presented options have to be evaluated. The required chip area has to be estimated in order to find the more area-efficient solution.

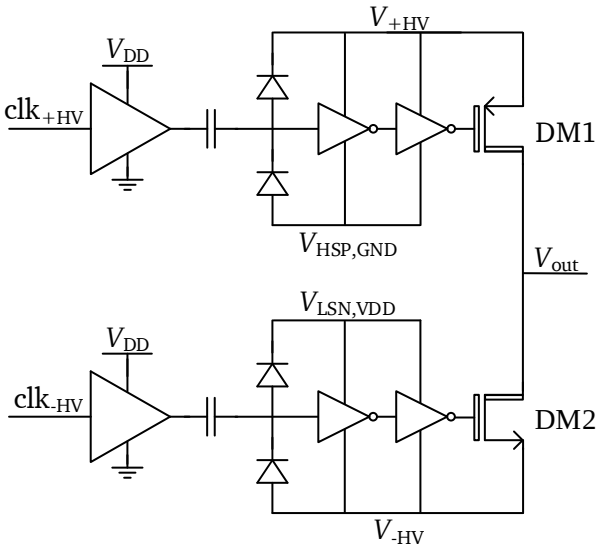


Figure 3.12.: AC coupled inverter with buffers for a high-side PMOS and a low-side NMOS transistor. The return-to-zero circuit is not shown.

3.2.1.2 Direct Coupling Level Shifter

Instead of passing the clock signals from the low voltage control to the high voltage output transistors by capacitors, the voltage levels can also be translated using resistive components which can withstand the voltage drop. The principle of this direct coupling topology is shown in Figure 3.13. The idea is to use transistor-based floating level shifters (FLS) that consume little power. The subsequent buffers or inverters work within the gate-source specification of the output transistors.

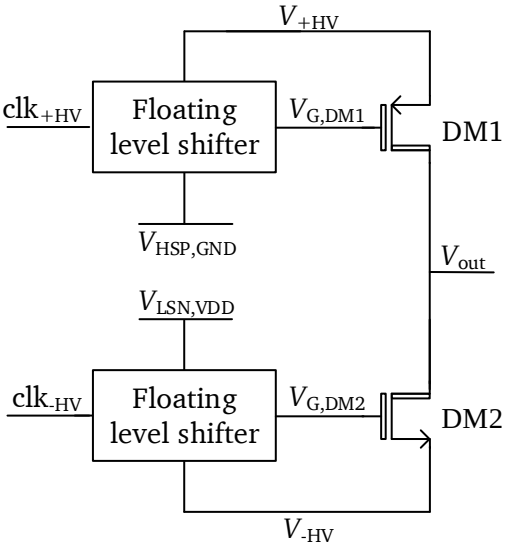


Figure 3.13.: DC coupled inverter for a high PMOS and a low NMOS transistor. The return-to-zero circuit is not shown.

Level shifters between two voltage domains are called floating level shifters. They can transform both, the low level and the high level into a different voltage domain. Different topologies for these level shifters are available. The basic principle is shown in Figure 3.14. Upon an input transition of $\mathrm{clk}_{+\mathrm{HV}}$ from low to high, the drain of transistor M1 is pulled to ground which results in a high V_{GS3} of transistor M3. As a consequence, the source potential of M5 has to increase to have a V_{GS5} higher than the threshold voltage of the PMOS so that a current can flow in this branch. A positive feedback by the cross-coupled transistors M7 and M8 enables a faster transition of the signal. The high-side output buffer or inverter is required to drive the high-side output transistor [70].

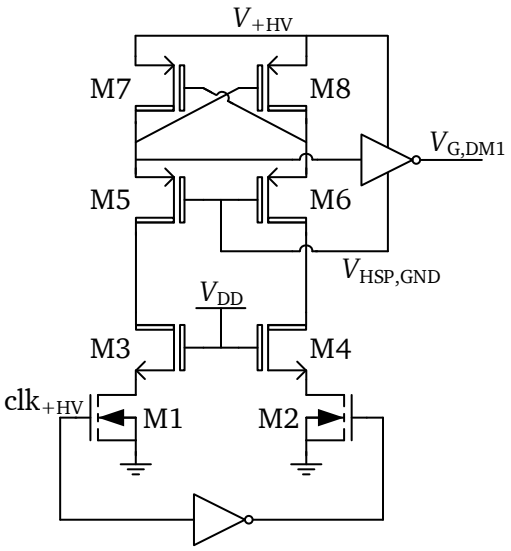


Figure 3.14.: Basic floating level shifter for a high-side PMOS transistor [70].

Instead of using an inverter to drive the high-side output transistor, a set-reset latch can be used. This minimizes the power consumption of the level shifter [71]. Another advantage of this topology is the fact that it can be adapted for the low-side NMOS gate driver. However, the level shifter requires six high voltage transistors, of which four have to be implemented as area consuming of p-type MOSFETs. For use in monolithic integrated inverters, the supply voltage of the driving buffers have to be generated on chip. The low level for the high-side PMOS transistor $V_{\mathrm{HSP,GND}}$ has to be maximum $V_{\mathrm{GS,max}}$ below the positive high supply voltage $V_{+\mathrm{HV}}$, whereas the high level for the low-side NMOS transistor $V_{\mathrm{LSN,VDD}}$ has to be maximum $V_{\mathrm{GS,max}}$ above the negative high supply voltage $V_{-\mathrm{HV}}$. The generation of $V_{\mathrm{HSP,GND}}$ and $V_{\mathrm{LSN,VDD}}$ add to the required chip area of the floating level shifter.

The HV7350 from Microchip Technology Inc. is an example of a commercially available three-state inverter with direct coupled topology. It is implemented in a high voltage CMOS process and can deliver peak currents of $\geq$1 A at up to ±60 V. The output waveform is a pulse signal with frequencies up to 20 MHz [72].

To apply this topology to a high-side NMOS transistor, the lower supply voltage $V_{\mathrm{HSN,GND}}$ is the output voltage of the inverter which is floating. Therefore, the gate has to be protected using zener diodes as shown in Figure 3.15. Again, for the level shifting of the excitation signal, high voltage PMOS transistors are required which consume much chip area.

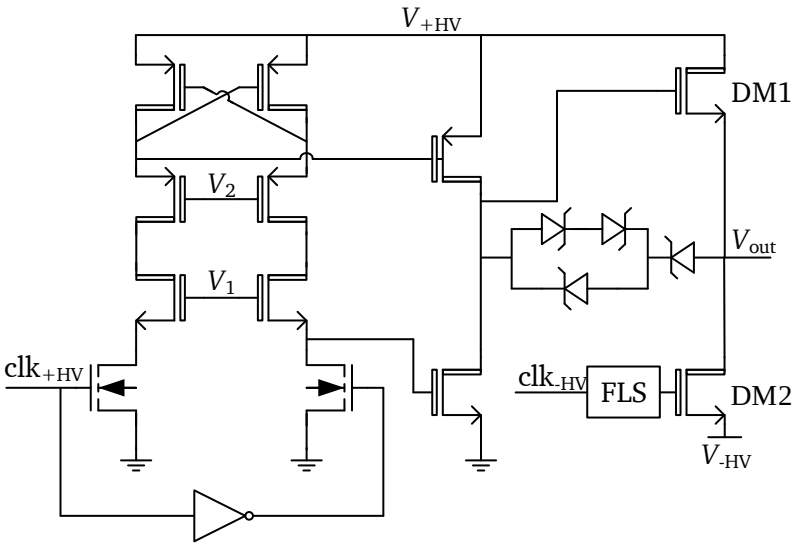


Figure 3.15.: Basic floating level shifter for a high-side NMOS transistor [73]. The floating level shifter for the low-side NMOS transistor can be implemented in an analogous approach to the presented high-side level shifter.

3.2.1.3 Bootstrapping Approach

Bootstrapping is popular method to generate the high voltage supply $V_{\mathrm{HSN,VDD}}$ within the gate-source specification for the gate voltage of a high-side NMOS transistor from its floating source terminal. A bootstrapping capacitor C_{Boot} is connected to the source of the high-side NMOS transistor and hence to the switching output of the inverter. It is charged via a diode to the requested gate-source voltage. For inverters with negative output voltages, the diode has to be connected to the a potential which is up to $V_{\mathrm{gs,max}}$ higher than the negative supply voltage $V_{-\mathrm{HV}}$. Hence, the on-voltage $V_{\mathrm{LSN,VDD}}$ of the low-side transistor DM2 is used to charge the bootstrapping capacitor. A level shifter and a buffer can transform the low level excitation signal to drive the high-side NMOS as shown in Figure 3.16.

The bootstrapping approach is widely used for the generation of the on-voltage $V_{\mathrm{HSN,VDD}}$ of the high-side output transistor DM1 within high voltage gate drivers. The bootstrapping capacitor, in general, is large in size since it has to deliver the current which is required to charge the gate of the large output transistor. Although some investigations have been made towards decreasing the size of the bootstrapping capacitor [74, 75], the area capacity for integrated high voltage capacitors is very low, which is why an integration of the bootstrapping capacitor is hardly feasible. Therefore, this approach is not suitable for full integration and not considered any further.

3.2.1.4 Return-to-zero Circuit

For high voltage applications it is mandatory to eliminate the charge stored on the capacitive load of the inverter upon request. This can be achieved by so-called return-to-zero (RTZ) circuitry. The charge on the load device can easily be transported to ground by an NMOS transistor connected to a diode for positive output voltages as shown in Figure 3.17a. A serial connected resistor can limit the current if the transition time can be increased. The lower peak current will reduce the size of the NMOS transistor for the RTZ transition. The diode is required to block the negative output voltages.

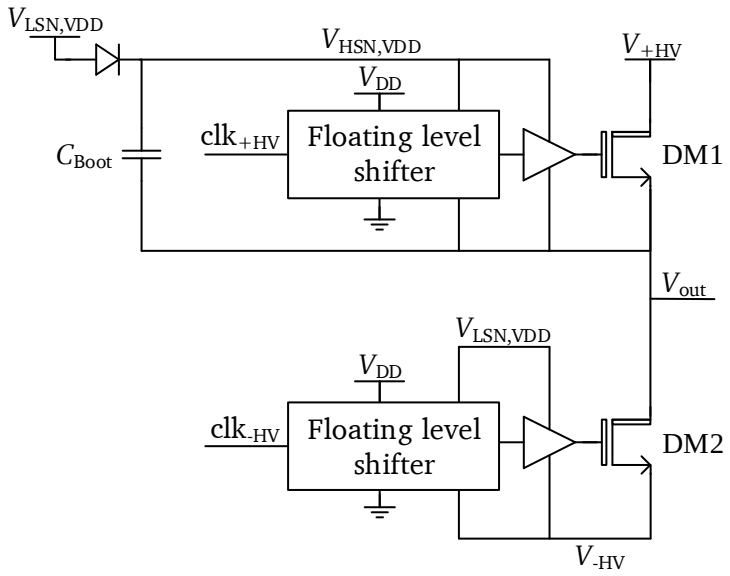
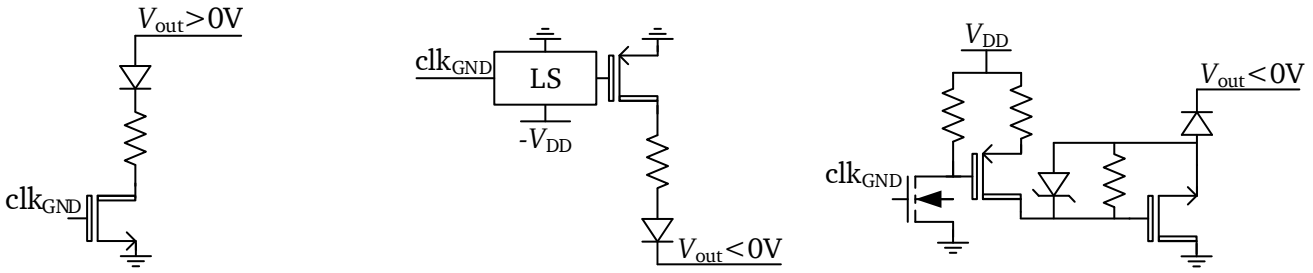


Figure 3.16.: Basic principle of bootstrapping for driving a high-side NMOS transistor based three-state inverter.



(a) RTZ from a positive high output voltage.

(b) RTZ from a negative high output voltage with a level shifter.

(c) RTZ from a negative high output voltage without negative low voltage supply.

Figure 3.17.: Schematic implementations for different return-to-zero architectures.

Returning to zero from a negative output voltage requires some more components. Analogous to the return-to-zero from a positive high voltage, the negative voltage can be eliminated by the circuit shown in Figure 3.17b. A negative low supply voltage and a subsequent level shifter is required to switch the PMOS transistor on which increases the complexity. If no negative supply voltage can be obtained, the transition can be achieved by the level shifting approach shown in Figure 3.17c.

3.2.2 Implemented Inverter

For the electroluminescent device described in section 3.1, a fully integrated three-state single ended inverter was designed. An SOI technology was chosen due to the reduced coupling for high voltages as explained in subsection 2.2.3. The chosen commercially available 1 µm BCD SOI technology for voltages up to 650 V is, inter alia, specially designed for driving capacitive loads such as EL devices. It offers low voltage bipolar and CMOS devices as well as HV DMOS transistors with breakdown voltages above 650 V within an SOI process. Besides, it offers high voltage diodes and special high resistive poly resistors as well as high voltage capacitors. The minimum structure size is 1 µm.

To compare the required chip areas of the HV PMOS and n-channel DMOS transistors, the slew rate (SR) was simulated and equalized at nominal simulations for p-type and n-type MOS transistors. The optimization was performed for the slew rate SR_{10-90} which can be calculated by the time difference of the output signal between 10 % and 90 % of the maximum output voltage. The slew rate for the NMOS is representing the falling edge whereas the positive edge is represented by the slew rate of the PMOS transistor. This procedure was simulated for the high voltage as well as for the available low voltage devices. The output load of the HV transistors was chosen to be equal to 10 nF which represents the maximum load of the inverter (see Table 3.1). For this comparison, the maximum high voltage was set to 100 V. The gate-source voltage was implemented ideally with a voltage drop of 5 V. Compared to the HV transistors, the maximum voltage for the low voltage devices was set to 5 V which equals the supply voltage V_{DD}. The load was chosen to be 100 fF which is a typical output load of digital circuits in the chosen technology. The size of the NMOS transistor was taken from the digital inverter cell with the minimum fan out.

Table 3.3 shows the comparison of the simulated slew rates for low voltage and high voltage transistors, respectively. It can be seen that the PMOS transistors were optimized to meet the slew rate SR_{10-90} of the corresponding NMOS transistor. For the obtained transistor sizes, the maximum slew rate SR_{max} for the PMOS implementation is higher than SR_{10-90}, both for low voltage and high voltage implementations. From this it can be concluded that the PMOS transistors, in sum, can deliver higher peak output currents than the NMOS transistors. However, second order effects such as channel length modulation, are more dominant in PMOS than in NMOS implementation which is why the difference between the maximum slew rate and SR_{10-90} is higher for PMOS compared to NMOS devices.

Table 3.3 also lists the required chip areas A for the transistors. It can be seen that the dimensions for the LV PMOS transistor requires a 2.66 times higher chip area than the LV NMOS transistor. This is due to the increased mobility of electrons compared to holes. To drive the same load with an equivalent slew rate in the high voltage domain, 26 PMOS transistors each of size 856.3x456 μm^2 have to be implemented. It can be concluded that the required area for a PMOS implementation of the high-side output transistor is 13.19 times higher than with a HV NMOS implementation. The large number of HV PMOS transistors also represents a high capacitance for the gate driver. To drive this load, a strong and thus area-intensive driver is required. Consequently, the required chip area for a PMOS implementation increase even more.

Table 3.3.: Comparison of the required chip area of LV and HV PMOS and NMOS transistors and corresponding slew rate for nominal simulations.

	LV		HV	
	NMOS	PMOS	NMOS	PMOS
$SR_{10-90}\left[V\,\mu s^{-1}\right]$	5821.0	5834.6	21.0	21.0
$SR_{max}\left[V\,\mu s^{-1}\right]$	6335.7	10963.7	24.0	30.3
Area A	7.4 x 8.7 μm^2	19.7 x 8.7 μm^2	0.77 mm^2	10.15 mm^2

The proportional higher difference between the required areas for the HV NMOS and HV PMOS compared to the low voltage devices can be explained by the structure of the DMOS transistors. While p-channel DMOS transistors in an n-doped SOI device wafer can only be built laterally, n-channel DMOS transistors can have an additional vertical current flow (see subsection 2.2.2). A vertical drift region can be added to the lateral drift regions by only a small increase in the required chip area as shown in Figure 3.18.

Since area is always an issue for IC design and is a main focus of the implementation within this thesis, the implementation of the high voltage pulse generator has to avoid HV PMOS transistors. Hence, the

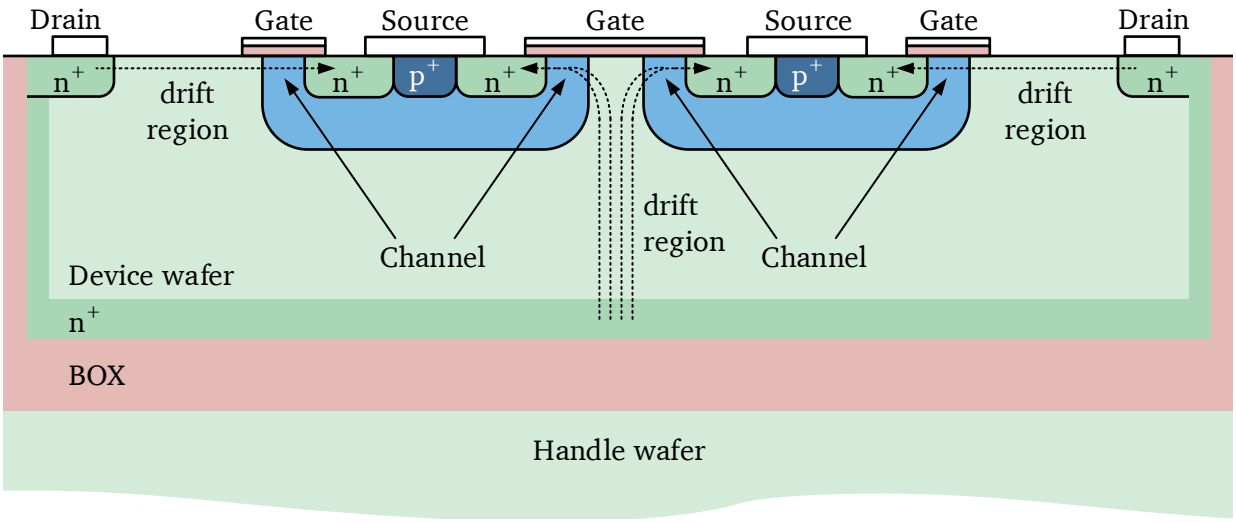


Figure 3.18.: Structure of an n-channel quasi-vertical DMOS transistor in an SOI technology (adapted from [13]).

high-side switch has to be implemented with an NMOS transistor resulting in a dual NMOS output stage. The AC coupling approach as well as the bootstrapping approach were not considered as the expected chip area is high as described in subsubsection 3.2.1.1 and subsubsection 3.2.1.3.

The direct coupling topology, described in subsection 3.2.1 and the level shifter shown in Figure 3.14, were implemented in the chosen technology. The required chip area for the high-side gate driver was estimated to 1.14 mm^2 which is 1.48 times larger than the high-side NMOS output transistor itself. This is due to the required high voltage PMOS and NMOS transistors within the level shifter. Even though the current in the level shifter is small, the minimum size of the high voltage transistors is large compared to low voltage transistors (compare Table 3.3).

Since integrated resistors that can withstand high voltages require less chip area than transistors, an open drain approach was considered for the implementation of the integrated inverter. Although resistive dividers consume more power than transistor implementations that only consume power during the switching event, it satisfies the focus of an area-efficient fully integrated solution. The schematic of the implemented ultra high voltage pulse generator is shown in Figure 3.19. The required chip area of the gate driver circuitry, without output transistors DM1, DM2 and DM3, is 0.29 mm^2 and thus is approximately 75 % smaller than the implemented direct coupling topology based on transistors within the floating level shifter presented in Figure 3.14.

The high-side NMOS transistor DM1 is normally turned off by a pull down resistor R_5 between its gate and the switching output V_{out} at its source. To turn it on, a low resistive path from the positive high voltage supply to the source is formed increasing the gate-source voltage. The input clock signal for the high-side switching clk_{+HV} is turned to the high level of the low voltage power supply V_{DD}. Consequently, transistor M1 turns on, pulling up the gate of transistor M2 to turn it on. Current can flow through R_3, M2 and R_2 to ground. Hence, the gate voltage of M3 reduces. The gate-source voltage is limited by the zener diode voltage of D1 which protects the gate oxide of M3 from breakdown. Hence, the high voltage drops across M2 which has to be implemented as a high voltage transistor. However, only the positive high voltage can drop across it and hence it only has to withstand V_{+HV} rather than the full output amplitude of $V_{+HV} - V_{-HV}$. If M3 is activated, a conductive path is formed from V_{+HV} to V_{out} and a voltage drop across

R_5 switches the output DMOS transistor DM1 on. As a consequence, the output voltage V_{out} rises to the positive high voltage power supply V_{+HV}. The gate-source voltage is limited by the zener diode D2 to protect the gate oxide.

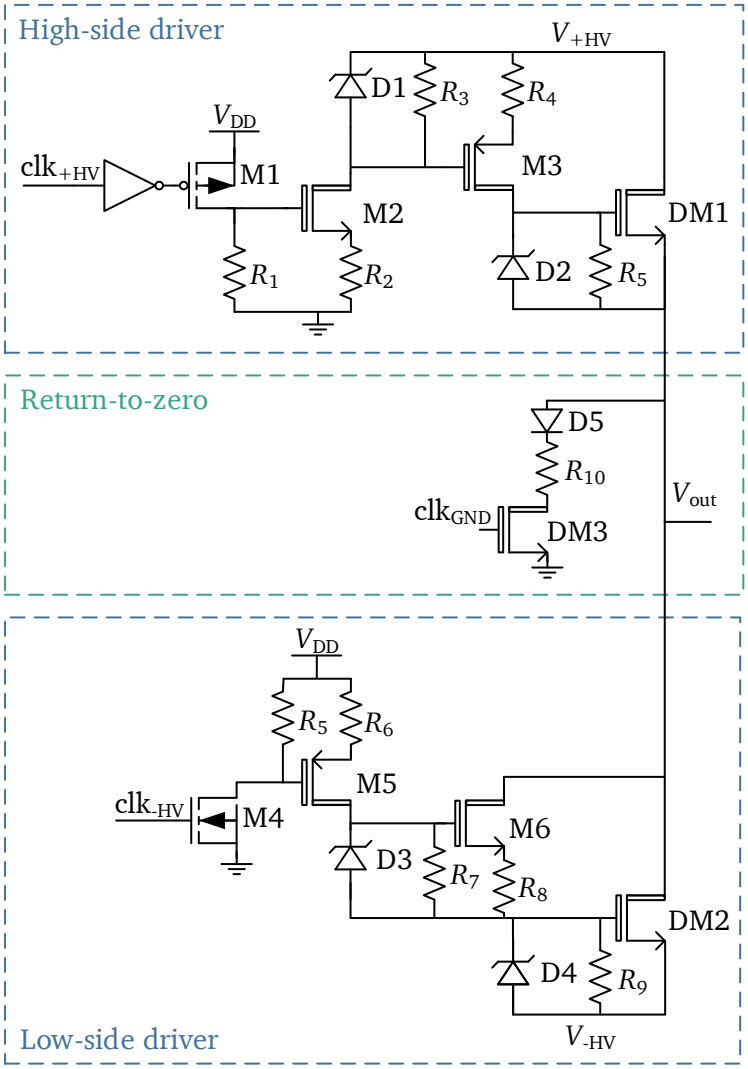


Figure 3.19.: Fully integrated high voltage pulse generator for capacitive loads.

If the input clock signal clk_{+HV} is set to zero, resistor R_1 pulls the gate of M2 to ground and turns it off. As a consequence, the gate of M3 is pulled to the high voltage power supply which stops current to flow on the gate of DM1. Due to R_5, remaining charge on the gate of DM1 is discharged and the transistor is turned off.

Subsequently, the low-side NMOS transistor DM2 can be turned on. A dead time between the clock signals for high-side and low-side driver prevents the circuit from cross currents between the positive and the negative high supply voltage. The implementation of the low-side NMOS gate driver is analogous to the high-side gate driver. To turn the low-side DMOS transistor on, the clock signal clk_{-HV} rises which turns transistor M4 on. The gate of M5 is pulled down which results in a current flowing through R_6 and M5 onto the gate of M6 which will then charge the gate of DM2. Consequently, the drain of DM2 is pulled towards the negative high supply voltage V_{-HV}. Transistor M6 was introduced for stability of the circuit. Furthermore, it uses the charge stored at the output V_{out} to charge the gate of DM2.

To be able to remove the charge stored on the output load at the third state, a return-to-zero circuit is implemented (see Figure 3.19). This type of RTZ can only be used after a positive high voltage due to the diode D5. A series resistor R_{10} limits the current in the RTZ branch which results in a smaller size of the transistor DM3.

The implemented inverter including the output transistors occupies a chip area of 1306.2 x 2152.9 μm^2. The output transistors DM1, DM2 and DM3 occupy a total chip area of 1.97 mm^2 which equals 70.07 % of the total inverter area.

To prevent short circuits within the high voltage inverter, a protection circuitry is implemented which drives the input transistors M4, DM3 as well as the inverter driving M1. It prevents current from flowing from one of the high supply voltage to either the other high voltage supply or directly to ground. If both input signals, in_{+HV} and in_{-HV} coming from an external controller are activated, the clock signals for the high-side and the low-side, clk_{+HV} and clk_{-HV}, are set to zero. The output of the inverter is therefore in a high impedance state. Furthermore, the short circuit protection circuitry delivers high output currents to drive the input transistors of the inverter. The schematic implementation is shown in Figure 3.20. A total chip area of 189.8 x 80.4 μm^2 is occupied by the short circuit protection.

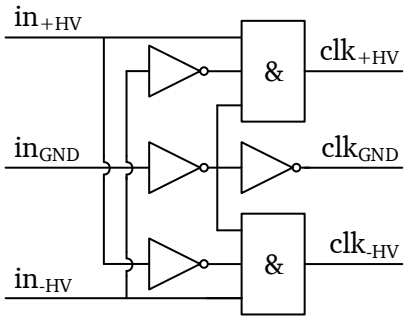


Figure 3.20.: Implemented short circuit protection for the clock signals of the high-side and the low-side driver as well as the return-to-zero circuit of the high voltage pulse generator.

3.3 Capacitive Sensor Excitation

Capacitive sensors can detect a capacitance or capacitance changes between two or more conductive objects [76]. The absolute capacitance is a function of the area of the conductors, their distance as well as the permittivity of the material between them. Hence, by capacitive sensing many physical properties such as pressure [77, 78], acceleration [79], humidity [80] and position [81, 82] can be determined. Thus, capacitive sensors are used in a wide variety of applications such as for example medical devices [83], automotive [84, 85] as well as consumer electronics [86]. Capacitive sensors gain interest since they require little power, can have a high sensitivity and in general have a simple structure [87, 82]. Due to these advantages, a capacitive sensor interface is chosen for detection of a stop request for the system presented in section 3.1.

According to [88], capacitive sensing measurements can be classified into three different modes: shunt, transmit and loading. Shunt mode generates an electrical field between a transmitter and a receiver, both of which are not grounded. Any grounded object reduces the energy stored in the electrical field between the two electrodes. In transmitting mode, an electrical field between transmitter and receiver is changed due to a conductive element [89]. Whereas shunt and transmit mode require two electrodes, loading mode is used whenever the second electrode is represented by the environment. A human, for example, consists of ionized water and thus has a conductivity to ground [89] and can represent the grounded

electrode. Due to its coupling to ground it can serve as the second electrode for capacitive sensors in loading mode. This measurement mode is explained in more detail since it is used in the presented application.

Figure 3.21 shows the principle of the loading mode capacitive sensing. A voltage is applied to a single electrode. An electrical field is formed to any surrounding ground potential. An approaching human hand represents the second, transmitting electrode, forming the sensing capacitor to ground. If the electrode in loading mode is driven with a peak voltage of V_p, the charge Q_sensor on the sensing capacitor changes due to the change of capacitance C_sensor according to

$$Q_\mathrm{sensor} = C_\mathrm{sensor} V_\mathrm{p}. \tag{3.1}$$

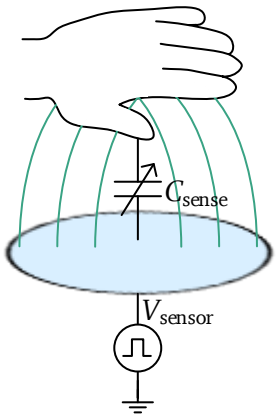


Figure 3.21.: Loading mode principle for capacitive sensors.

In 2010, the use of spread spectrum techniques for capacitive sensors was introduced for the first time [56]. This method turned out to be highly sensitive which is why it is most suitable for robust sensor operation in harsh environments. Due to the spreading of the bandwidth, interferences with a small frequency range are attenuated and do not cause any unwanted triggering of the capacitive sensor [90]. Furthermore, the radiated signal can comply with electromagnetic compatibility standards. Because of these advantages, a spread spectrum approach for the capacitive sensor excitation was chosen for the presented application. The spread spectrum technique will be discussed in more detail in the following subsection. Afterwards, the implementation of a spread spectrum clock generator is presented.

3.3.1 Spread Spectrum Clock Generator Concepts

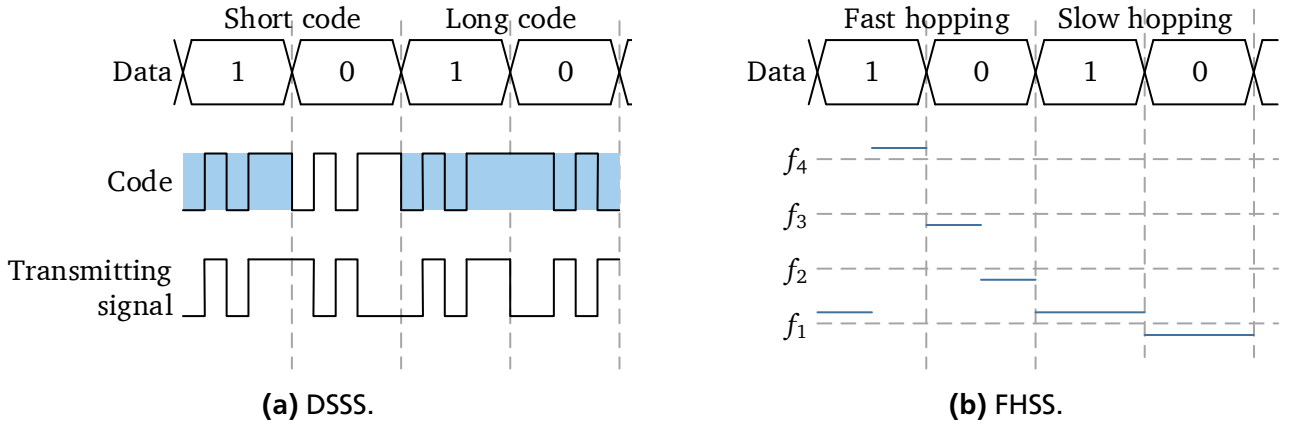
An important task of telecommunications is to transmit information without interference from a transmitter to a receiver. For this purpose, the so-called spread spectrum method was originally developed. In this case, narrow-band information is transmitted by expanding the transmission bandwidth. The signal spectral density is thereby reduced and the signal is lost in the environmental noise. By a random or pseudo-random change of the spreading code, the information can be hidden from unwanted recipients [91].

Besides others, two methods have emerged, the direct-sequence spread spectrum (DSSS) and frequency-hopping spread spectrum (FHSS). However, they share the idea of a wide transmitting frequency band. For transmission, the information is modulated twice. First, the information is modulated in the narrow data-band spectrum using frequency shift keying (FSK), phase shift keying (PSK) or amplitude shift keying (ASK). Subsequently, the spreading of the transmission spectrum takes place.

For DSSS the data is modulated using a spreading code. This code has a higher bandwidth than the actual data. The modulation can be realized, for example, with an XNOR gate as shown in Figure 3.22a. A

distinction is made between a short code and a long code transmission, wherein in short code a data bit is modulated with the entire spreading code, while in long code several data bits are transmitted per spreading code [92].

In the FHSS, the carrier frequency of the transmission is changed pseudo-randomly, so that the data is transmitted at different frequencies as shown in Figure 3.22b. This divides the available bandwidth into N channels. Compared to DSSS, the bandwidth can be implemented much wider with FHSS. Analogous to DSSS, there are also two hopping methods. For fast hopping, several frequencies are used per data packet, while for slow hopping several data packets are distributed over one frequency. This technique was chosen for the application described in section 3.1.



(a) DSSS. **(b)** FHSS.

Figure 3.22.: Data transmission for the two main spread spectrum methods: direct-sequence spread spectrum and frequency-hopping spread spectrum (adapted from [92]).

Figure 3.23 shows the block diagram of an FHSS system with transmitter and receiver. The channel in between can be noisy and hence introduce influencing signals onto the transmitted signal. Narrow-band signals will only influence if they occur at the time when data is transmitted at a similar frequency and will be attenuated at all other times. The demodulation on the receiver side can be implemented if the pseudo-random number (PRN) code is known.

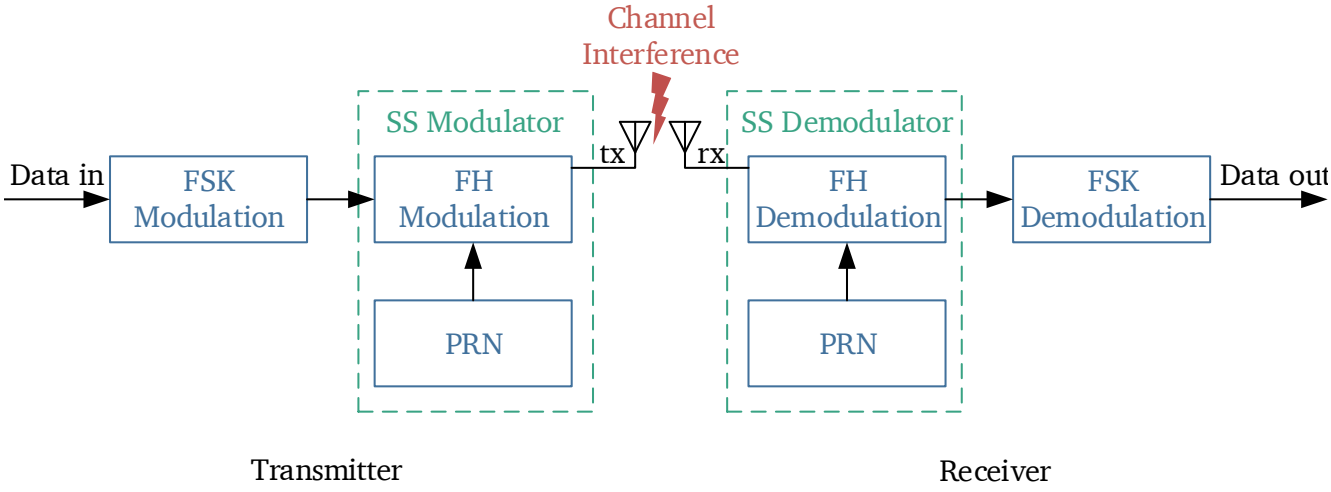


Figure 3.23.: Block diagram of an FHSS system for data transmission (adapted from [91] and [92]).

Although the spread spectrum technique has been introduced in telecommunications, it finds favor in other applications due to the reduction of signal power such as for example electromagnetic interference (EMI) reduction in switching regulators [93], linear drop-out regulators [94] and capacitive sensing [56].

When using the spread spectrum technique for capacitive sensing, a substantial difference arises compared to data transmission in communication systems. The transmitter is not supposed to transmit any data. Instead, the spread spectrum modulation frequency is directly fed into the sensing electrode and hence a signal is provided to sense the influences of the sounding environment. Instead of suppressing any disturbances within the channel, the influences of the channel are the signal to be detected.

3.3.2 Implemented Spread Spectrum Clock Generator

The design of the spread spectrum clock generator was inspired by the example in [95] which was adapted to the specifications given in Table 3.2. The block diagram is presented in Figure 3.24. It is based on a relaxation oscillator (RC-oscillator) which consists of a capacitor C_{SSCG} that is charged by a current source. When the voltage across the capacitor reaches a defined value, a comparator changes its output. The capacitor is discharged within a short time by a parallel connected transistor.

The basic principle of the implemented SSCG is that a pseudo-random number is converted into an analog voltage which is then transduced into a current. This current charges a capacitor. The voltage on the capacitor is compared to a reference voltage. A digital logic generates the output signal V_{SSCG} with a duty cycle of 50 %. In the following, the schematic implementations of the different building blocks within the SSCG are explained in more detail.

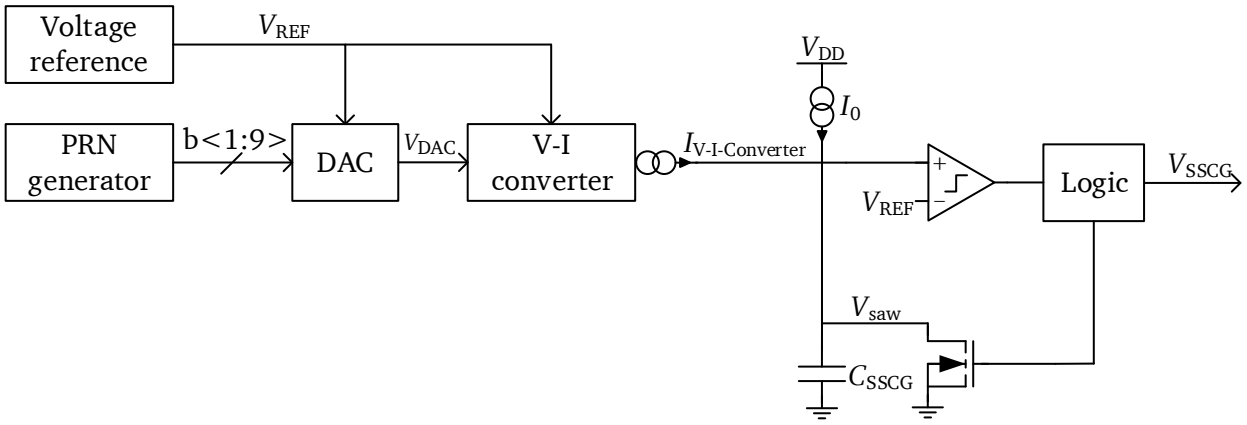


Figure 3.24.: Block diagram of the implemented spread spectrum clock generator.

3.3.2.1 Implemented Voltage Reference

A voltage reference is implemented to obtain an on-chip reference voltage. This voltage represents the maximum voltage of the digital-to-analog converter, the reference voltage for the voltage-to-current conversion as well as for the comparator within the oscillator logic which creates the digital output signal.

A bandgap is implemented with a design taken from [96, p. 159]. The schematic implementation is shown in Figure 3.25. The bandgap voltage V_{BG} is fed into a non-inverting amplifier to obtain a stable output voltage V_{REF} of 3.5 V. The reference voltage V_{REF} is stabilized with an on-chip capacitor C_1 of 1.14 pF. It occupies a chip area of 309.2 x 460.2 $\mu\mathrm{m}^2$.

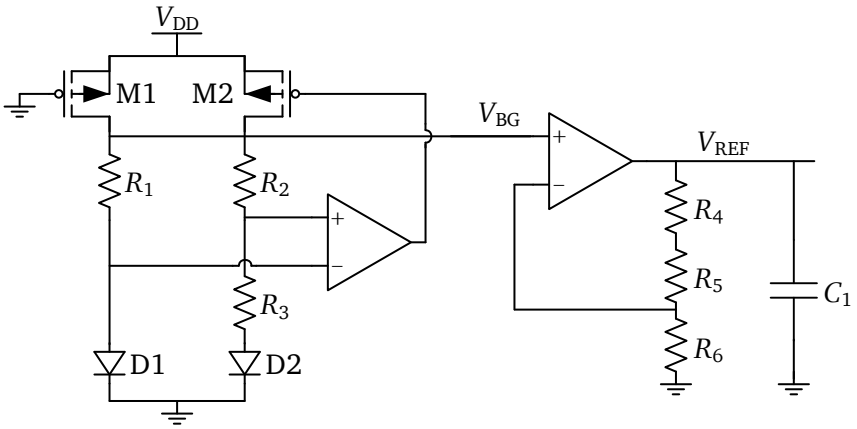


Figure 3.25.: Schematic of the implemented bandgap.

Figure 3.26 shows the output voltage V_{REF} of the voltage reference. Over the complete temperature range of -40 °C to +80 °C the maximum deviation of the nominated post-layout simulation is 39.10 ppm/K. For the worst power (wp) corner the temperature coefficient is 74.76 ppm/K. The maximum simulated temperature dependence is 85.63 ppm/K for the worst speed (ws) corner.

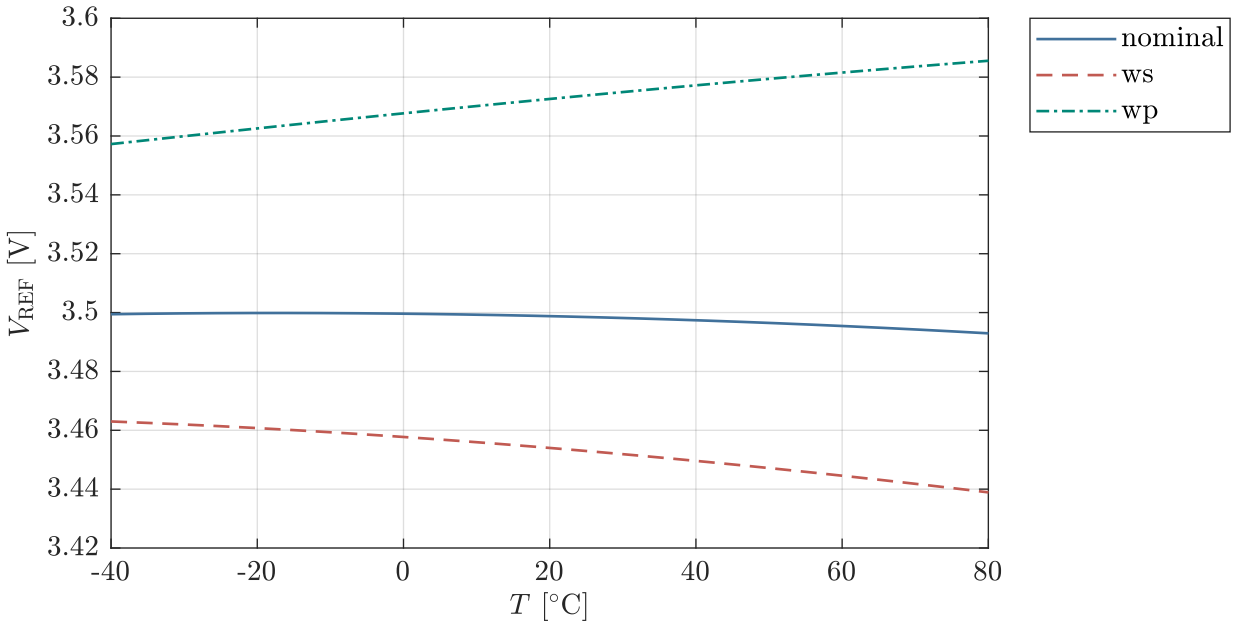


Figure 3.26.: Output voltage V_{REF} of the voltage reference for post-layout simulations.

The resistances in the non-inverting amplifier R_4, R_5 and R_6 are implemented as high resistive with a value of 52.91 kΩ. However, the output resistance of the bandgap reference is reduced to drive connected circuits due to wide output transistors within the operating amplifier. The output resistance is only 201.57 Ω for nominal post-layout simulation. It increases to 326.47 Ω for worst speed corner at +80 °C as shown in Figure 3.27.

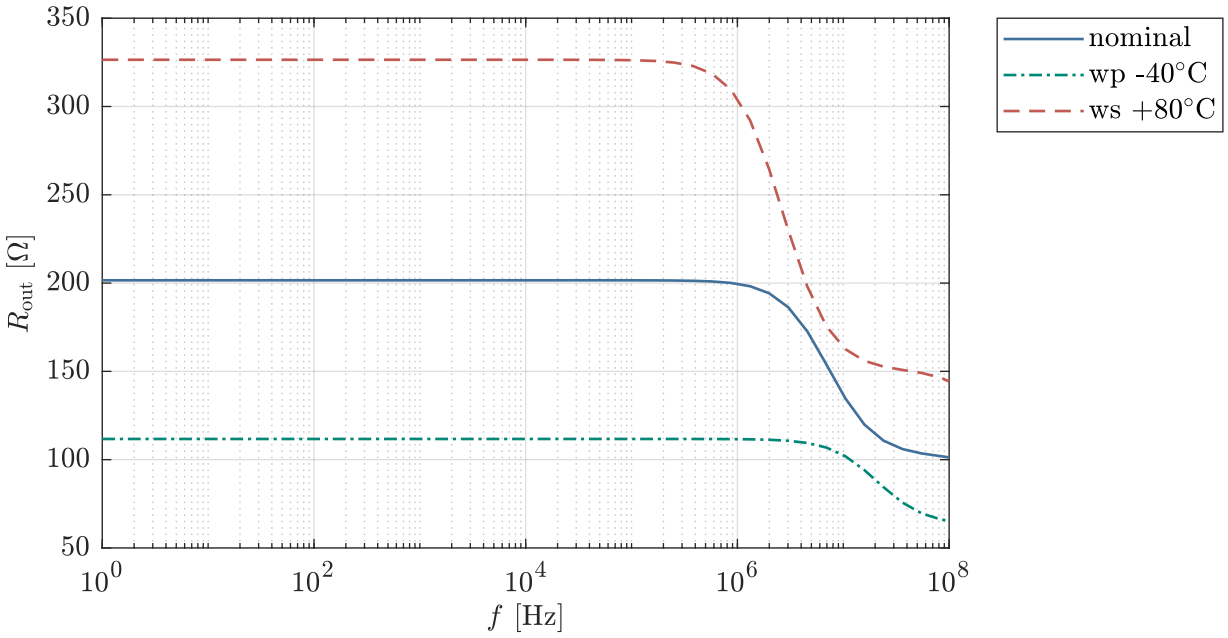


Figure 3.27.: Output resistance R_{out} of the voltage reference for post-layout simulations.

3.3.2.2 Implemented Pseudo-random Number Generator

A pseudo-random number is used to hop between the frequencies of the SSCG in a pseudo random pattern. This reduces the influences of narrow band interfering signals. It is implemented with a linear-feedback shift register (LFSR). The register consists of series connected flip-flops and has a length of nine bit according to the required resolution. The output of the LFSR can be described by a primitive polynomial, which has a maximum amount of different output states with the least number of polynomials. The maximum length of the LFSR is $2^{\text{N}} - 1$. The powers of the polynomials occurring in the primitive polynomial are the values of the registers whose outputs are fed to an XNOR gate. The output of the feedback gate is connected to the input of the first register. According to [97], the primitive polynomial is

$$p(x) = x^9 + x^5 \tag{3.2}$$

and hence the outputs of the fifth and the ninth flip-flops are used for the feedback. The schematic implementation is shown in Figure 3.28.

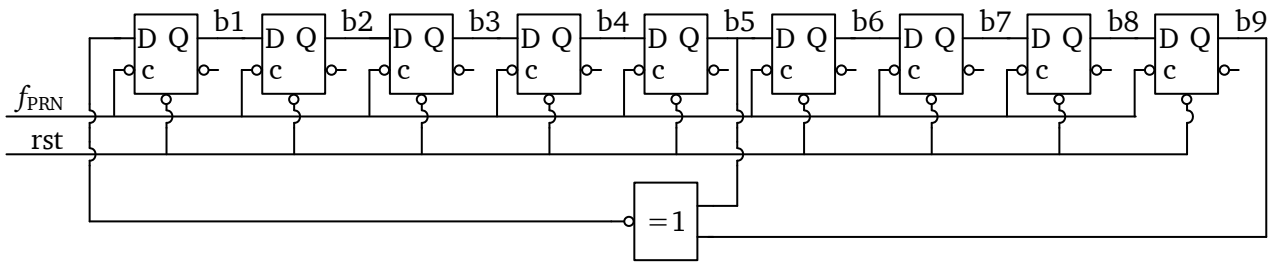


Figure 3.28.: Schematic of the implemented pseudo-random number generator.

At start-up, the flip-flops are reset to the decimal value '0' which represents the seed value for the LFSR. It enables a maximum length of the PRN. If the sensor is activated, a clock signal is given to the flip-flop and the output of the XNOR gate is processed to the output of the flip-flop. This procedure is executed until

the decimal starting value '0' is detected again. At that point, the pseudo-random number generator stops generating new values until the sensor is activated again.

The frequency f_{PRN} with which new PRN are generated can be determined by the resolution N_{PRN} of the spread spectrum and the overall sweep time of the sensor t_{sensor} to

$$f_{\mathrm{PRN}} = \frac{2^{N_{\mathrm{PRN}}}}{t_{\mathrm{sensor}}} = \frac{512}{8\,\mathrm{ms}} = 64.00\,\mathrm{kHz}. \tag{3.3}$$

The stored content of the flip-flops (b1 to b9) is used as the input of the digital-to-analog converter. The implemented PRN generator occupies an area of 358.5 x 107.6 μm^2.

3.3.2.3 Implemented Digital-to-Analog Converter

The digital-to-analog converter converts the digital number from the PRN generator to an analog output voltage which can be used to tune the charging current for the capacitance C_{SSCG} of the RC-oscillator, as explained in subsection 3.3.2. The architecture of the DAC was chosen as an R2R-ladder since it enables DC stable output voltages. In the laboratory, as well as in later use, this allows the output voltage of the DAC to be maintained over a long period of time, thus stopping the oscillator at a certain frequency.

The resolution of the DAC is 9 bit which is given in the specification of the spread spectrum clock generator (see Table 3.2). The maximum output voltage of the DAC was set to the reference voltage V_{REF}. The regulated voltage reduces noise of the DAC output voltage caused by supply voltage variations. In addition, the subsequent voltage-to-current (V-I) converter works with an input voltage range of 0 V to 3.5 V whereby a sufficiently large drain-source voltage V_{DS} results for the used PMOS transistors used in the subsequent stage. Hence, p-channel transistors which charge the capacitance of the oscillator work in saturation. For the DAC, a voltage of

$$V_{\mathrm{LSB}} = \frac{V_{\mathrm{REF}}}{2^N} = \frac{3.5\,\mathrm{V}}{2^9} = 6.84\,\mathrm{mV} \tag{3.4}$$

results for the least significant bit (LSB).

The R2R-ladder consists of resistors and switches, which are both possible sources of errors. Layout techniques can be used to minimize mismatch influences within the design [98]. However, manufacturing tolerances of the resistors can not be influenced. In contrast, influence of the switches can be reduced by the design. In order to minimize the influence of the switches, on the one hand, the absolute values of the implemented resistors R of the R2R-ladder can be increased. This, in turn, increases the chip area. On the other hand, the transistors can be implemented with large widths which reduces the on-resistance of the switches. Since the switches are required for every bit of the DAC, the required chip area for all switches is proportional to the resolution of the DAC. Instead of increasing the transistor sizes of the buffer for every bit, the on-state resistance of the switches can be regulated [99, 100].

This concept allows the reduction of the switch size at the expense of a regulating circuit and is followed in this thesis. The idea of the switch compensation is explained using a non-ideal most significant bit (MSB) being '1' whereas all other bits are assumed to be grounded having ideally matched output buffers. This assumption can be made since variations of the output buffer of the MSB have the highest impact on the output voltage of the DAC [101]. The equivalent circuit of the R2R-ladder is shown in Figure 3.29. The output resistance of the switch R_{switch} represents an offset to the series resistance $2R$ and thus distorts the output voltage of the DAC. For a specific operating point, this error can be compensated by reducing the value of the series resistor $2R$ by $R_{\mathrm{switch,op}}$ or by increasing the value of R to $R + R_{\mathrm{switch,op}}$. However, the

output resistance of the switch changes due to process as well as temperature variations. The difference of the actual resistance R_{switch} from the value at the operating point $R_{\text{switch,op}}$ will be referred to as Δr_{switch} and is given by

$$\Delta r_{\text{switch}} = R_{\text{switch,op}} - R_{\text{switch}}. \tag{3.5}$$

The compensation circuit minimizes the influences of Δr_{switch} by regulating the gate-source voltage of the transistors within the output buffer of each bit of the DAC.

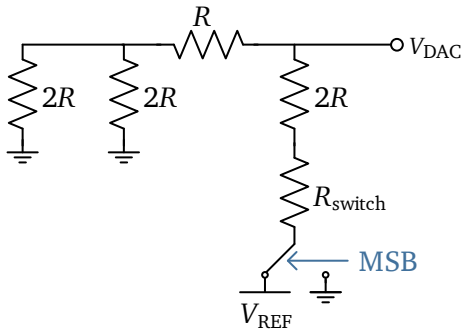


Figure 3.29.: Equivalent circuit for the explanation of the switch compensation. The switch for the MSB is non-ideal whereas all other bits are grounded ideally.

From Figure 3.29, the output voltage v_{DAC} as well as its deviation due to the output resistance of the switches can be calculated. The deviation of the output voltage for the MSB $\Delta v_{\text{DAC,MSB}}$ from the ideal output voltage of $0.5 \cdot V_{\text{REF}}$ is

$$\Delta V_{\text{DAC,MSB}} = \left(\frac{1}{2 + \frac{\Delta r_{\text{switch}}}{2R}} - \frac{1}{2} \right) V_{\text{REF}}. \tag{3.6}$$

It can be seen that the error of the output voltage $\Delta V_{\text{DAC,MSB}}$ reduces if the value of R is increased. However, this increases the required chip area. Instead, Δr_{switch} can be reduced by either increasing the width of the buffer output transistors which also adds chip area for every single bit or by regulating the output resistance [99, 100].

The regulation approach was chosen in the presented design and was realized by defined gate-source voltages of the p- and n-channel transistors of the switches. The on-voltages of the PMOS and NMOS transistors are referred to as V_{P} and V_{N}, respectively. V_{P} and V_{N} are chosen so that all PMOS and NMOS switch transistors of the 9 bits are operating in the linear region.

The switches for driving the resistor ladder of the R2R-ladder DAC are implemented by a CMOS output stage and inverting level shifters to drive the NMOS as well as for the PMOS transistor as shown in Figure 3.30. The inverting level shifters are connected to V_{DD} and V_{P} as well as to V_{N} and ground for the PMOS and NMOS transistor, respectively.

The voltages V_{P} and V_{N} are obtained by a regulating circuit shown in Figure 3.31. To ensure a linear operating region for M3 and M4, R_1 is chosen much smaller than R_2. The output resistance r_{out} of M3 and M4, respectively, can be calculated by the relation of the implemented resistances R_1, R_2 and R_3 by

$$\frac{R_1}{2R_1 + R_2} = \frac{R_3}{2r_{\text{out}} + R_3} \tag{3.7}$$

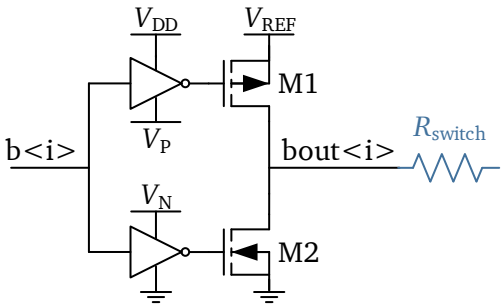


Figure 3.30.: Schematic implementation of the switches within the DAC for driving the resistors in the R2R-ladder DAC with i being the bit number.

which can be transformed for r_{out} to

$$r_{out} = \frac{1}{2}\left(\frac{R_3\,(2R_1 + R_2)}{R_1} - R_3\right). \tag{3.8}$$

This output resistance will also be achieved for M1 and M2 within the switch of the DAC shown in Figure 3.30 if their W/L-ratios match to the transistor sizes with the regulation circuit M3 and M4, respectively.

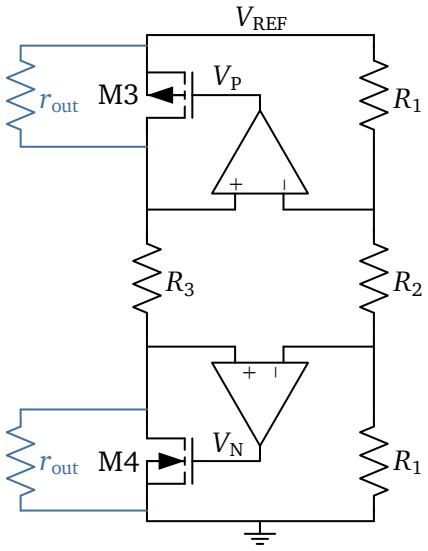


Figure 3.31.: Regulation circuit to reduce the output resistance deviations Δr_{out} of the buffer MOSFETs which are shown in blue.

To verify the switch compensation regulation, three systems with comparable switch and resistor sizes were investigated by simulations. First, an R2R-ladder DAC without switch compensation was implemented. The second system presents the fabricated DAC whereas the third system represents an improvement of the fabricated version.

The benefit of the regulation circuit is the reduction of the output resistance variations of the switches Δr_{switch} compared to the nominal value $R_{switch,op}$. Simulations were performed for all corners, supply voltage variations of ±10 % and temperature changes from -40 °C to +80 °C. Table 3.4 shows that the ratio of the maximal deviation of the output resistance of the switches $\Delta r_{switch,max}$ to $R_{switch,op}$ can be reduced due to the regulation by a factor of 8.5 for the system with the improved regulation. Likewise,

Table 3.4.: Simulated characteristics of three comparable DAC implementations for all corners, supply voltage changes of ±10 % and temperature variations from -40 °C to +80 °C.

Implementation	$\left\lvert\frac{\Delta r_{\text{switch,max}}}{R_{\text{switch,op}}}\right\rvert$ [%]	|DNL| [LBS]
Without regulation	2.72	4.02
With regulation	0.09	1.22
Fabricated DAC	0.78	7.09

the differential non linearity (DNL) error reduces by 69.65 % due to the regulation circuitry. This proves the concept of the switch regulation.

In the implementation of the presented SoC, the DAC was not characterized in detail. Instead, the focus was put on the output characteristic of the complete SSCG. The output frequency f_{SSCG} has been optimized for linearity. Only with later characterization of the DAC, it was noticed that M1 from Figure 3.30 was chosen too large compared to M3 of Figure 3.31. Therefore, the output resistance of the switches were not optimally fitted to the resistors of the R2R-ladder of the DAC. Furthermore, R_1 was chosen too small with respect to R_2 which resulted in low input voltage ranges for the operational amplifier generating V_{N}. Hence, the regulation circuit does not work for all corners, temperature ranges and supply voltage variations. As a consequence, the output resistance deviation as well as the DNL of the buffer is higher for the implemented DAC than for the improved implementation across all corners as well as supply voltage and temperature changes as shown in Table 3.4. The deviation of the process production thus has a considerable influence on the characteristic curve of the DAC when changing the MSB. However, due to the pseudo-random pattern, the DNL error of the DAC does not influence the system performance of the SSCG. Only a slight variation of the output spectrum can be expected if the DNL is higher than one LSB for the fabricated SoC.

The implemented DAC occupies a chip area of 291.8 x 1261.5 μm^2. The regulation circuitry occupies an area of 243.3 x 533.3 μm^2 which equals 35.25 % of the DAC area. The output of the DAC is connected to a voltage-to-current converter which generates the current for the RC-oscillator.

3.3.2.4 Implemented Voltage-to-Current Converter

The output voltage of the DAC is converted into a current which is then used to charge the capacitance of the RC-oscillator. The schematic of the voltage-to-current converter is shown in Figure 3.32. The basic idea is that the voltage at the differential input of the first stage is kept at the reference voltage causing a voltage drop across and hence a current through resistor R. This current i_{out4} flows through transistor M11 and M12 and is mirrored to the load capacitance of the oscillator.

The circuit consists of four stages. The first stage is a differential amplifier. One input is connected to the reference voltage V_{REF}, whereas the second input is connected to a resistor. The amplifier tries to maintain the reference voltage at the negative input which results in a voltage drop across the input resistor R. Therefore, a current of

$$i_{\text{R}} = \frac{V_{\text{REF}} - v_{\text{DAC}}}{R} \tag{3.9}$$

is generated. The differential output of the first stage is mirrored to a high amplification gain stage. The load of this second stage is a cascode current mirror which represents the third stage due to the feedback

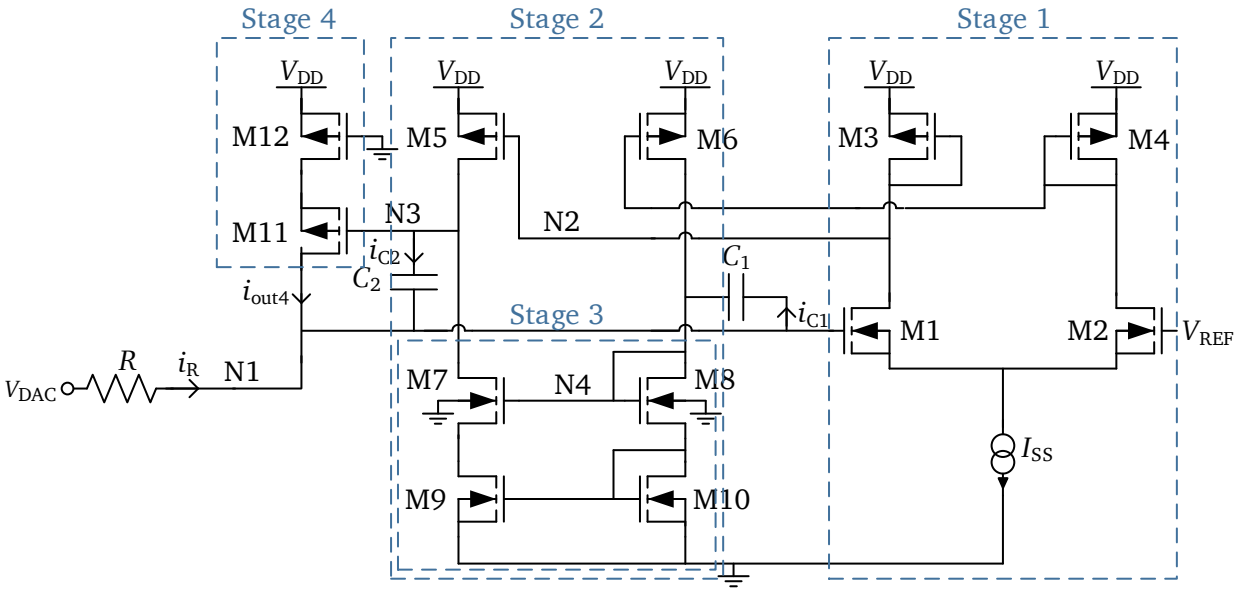


Figure 3.32.: Schematic of the implemented voltage-to-current converter.

C_2 at the positive output. The positive output of the second stage is connected to the fourth stage, a single stage amplifier with source degeneration. The current through the output transistor of stage four, M11, is equal to the input current i_R and is mirror to load the capacitance of the RC-oscillator.

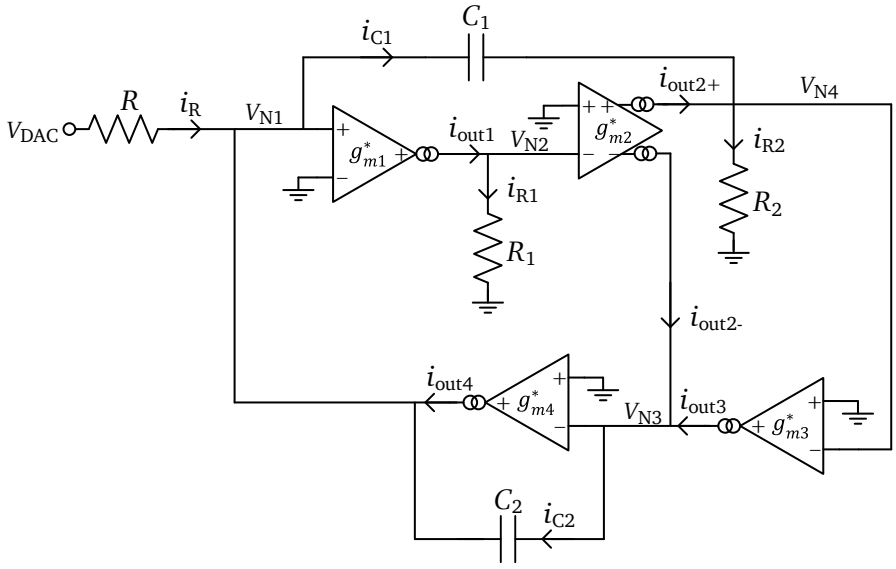


Figure 3.33.: Simplified small signal equivalent circuit to derive the transconductance of the voltage-to-current converter.

To derive the transconductance of the voltage-to-current converter, the small signal equivalent circuit can be represented as shown in Figure 3.33 with simplifications described in the following. All amplification stages are modeled as voltage to current conversions with a transconductance g^*_{mi} with i being the number of the stage.

The first input stage is a differential input stage consisting of M1 and M2 as the differential input pair and M3 and M4 as diode connected loads. Due to its fully symmetrical design, the calculations can be performed regarding a single branch and splitting the input into a differential signal of $\pm v_{id}/2$. The

transconductance of this first stage g^*_{m1} equals half of the transconductance of the input transistor M1 and M2

$$g^*_{m1} = 0.5 g_{m1,2}. \tag{3.10}$$

The impedance at the output of the first stage R_1 is dominated by the diode connection of the load transistors M3 and M4 with a resistance of

$$R_1 = \frac{1}{g_{m3,4}}. \tag{3.11}$$

The second stage, consisting of M5 to M10, adds another amplification and performs the transformation from differential to single ended. The positive output is connected to the low impedance input of a cascode stage, R_2, which is dominated by the diode connection of the identical transistors M8 and M10 and can be determined by

$$R_2 = \frac{2}{g_{m8,10}}. \tag{3.12}$$

The positive output of the second stage adds negative feedback to the input stage by the feedback capacitor C_2. The transconductance of the second stage is given by the transconductance of the input transistors M5 and M6 by

$$g^*_{m2+} = x g^*_{m2} = g_{m5} = \frac{g_{m6}}{x}, \tag{3.13}$$

if the widths of the transistors are weighted with a factor x, $W_6 = x W_5$. The negative output of this stage is connected to the gate of the output transistor M11. Due to the high output impedance of the cascode current mirror load and the high output impedance of the input transistor M5, the output impedance at the negative output of stage two (node N3) can be neglected.

Although the cascode current mirror (M7 to M10) is not intended to be used as an amplifier, the required negative feedback of C_2 can add input signal from node N1 to the gate potential of the cascode current mirror. Consequently, this change is amplified and a current is added to node N3 which is the input of the output stage. The transconductance of stage three g^*_{m3} is given by

$$g^*_{m3} = \frac{1}{x R_2} \tag{3.14}$$

since the current in the input impedance of the current mirror is amplified to its output. Again, the output impedance of this stage is represented by the high output impedance of the cascoded current mirror in parallel to the high output impedance of M5 and is therefore neglected.

The fourth stage, consisting of M11 and M12, is a common source amplifier with source degeneration. The amplification transistor M11 has to be sized so that it always works in saturation. The transconductance of this stage is given by transistor M11 and the on-resistance of M12 by

$$g^*_{m4} = \frac{g_{m11}}{1 + r_{on12} g_{m11}}. \tag{3.15}$$

The output impedance of this stage can be neglected due to the low impedance of the input resistance R. A Miller capacitance is connected between the gate and the drain of M11 to decrease input impedance. The output current of this stage is mirrored to the capacitance of the RC-oscillator. Therefore, the transconductance of the voltage-to-current converter can be derived by the current through M11 divided by the input voltage V_{DAC}.

The derivation of the transconductance of the voltage to current $g_{\mathrm{V-I-converter}}$ converter can be found in Appendix B. It is given by

$$g_{\mathrm{V-I-converter}} = \frac{i_{\mathrm{out4}}}{v_{\mathrm{DAC}}} = \frac{g^*_{\mathrm{m4}}\left(g^*_{\mathrm{m}} + sC_2\right)}{sC_2Z^*_{\mathrm{N1}} + R\left(sC_2 + g^*_{\mathrm{m}}sC_2Z^*_{\mathrm{N1}} + g^*_{\mathrm{m4}}sC_2Z^*_{\mathrm{N1}}\right)} \tag{3.16}$$

with

$$g^*_{\mathrm{m}} = \frac{i_{\mathrm{C2}}}{v_{\mathrm{N1}}} = 2g^*_{\mathrm{m1}}g^*_{\mathrm{m2}}R_1 - \frac{\frac{1}{x} + g^*_{\mathrm{m1}}g^*_{\mathrm{m2}}R_1R_2}{R_2 + \frac{1}{sC_1}} \tag{3.17}$$

and

$$Z^*_{\mathrm{N1}} = Z_{\mathrm{N1}} \| \frac{1}{sC_{\mathrm{in}}} = \frac{R_2 + \frac{1}{sC_1}}{1 + xg^*_{\mathrm{m1}}g^*_{\mathrm{m2}}R_1R_2} \| \frac{1}{sC_{\mathrm{in}}}. \tag{3.18}$$

A parallel capacitance C_{in} from node N1 to ground is assumed due to the large size of the input resistor R with low thermal temperature coefficient.

Figure 3.34 shows the transconductance of the V-I converter in the relevant frequency range. The calculation shows good conformity of calculation and SPICE simulations for frequencies up to 40 MHz. For higher frequencies, input capacitances, input resistances as well as so far neglected output resistances come into account.

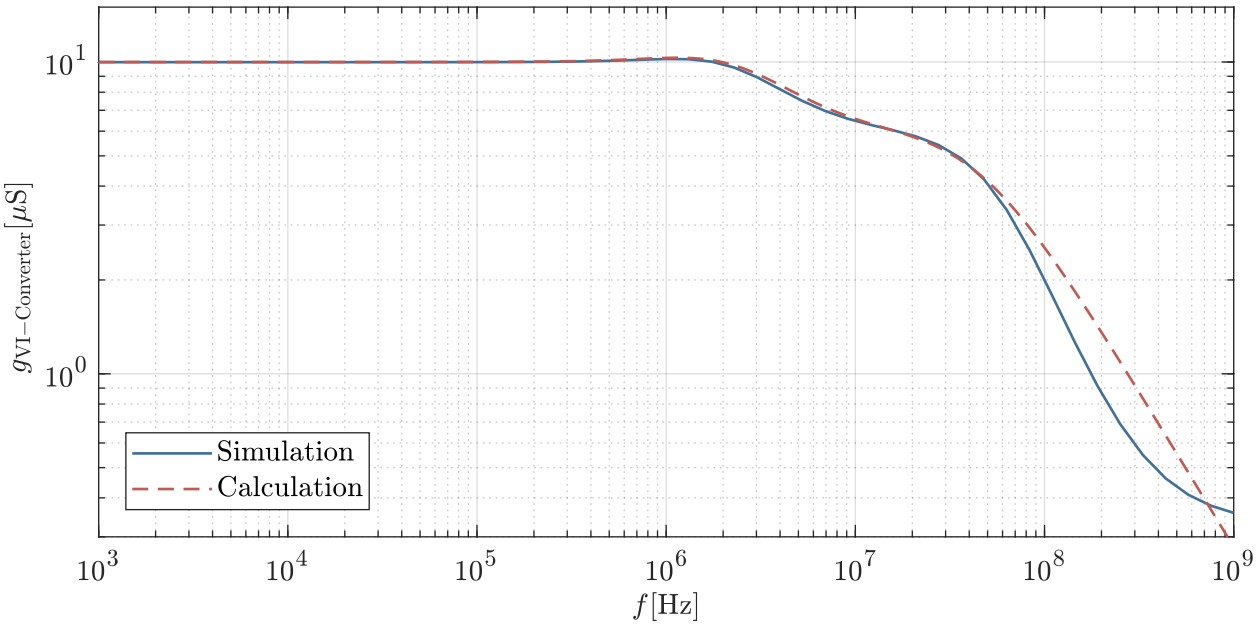


Figure 3.34.: Simplified small signal equivalent circuit to derive the transconductance of the voltage-to-current converter.

The output current of stage four i_{out4} is mirrored to the capacitance of the RC-oscillator. Due to the oscillation of the voltage across the capacitance between ground and V_{REF}, a large signal effect occurs. Figure 3.35 shows the block diagram of the output current mirror which drives the capacitance of the RC-oscillator. Due to the oscillation, the drain voltage of the output transistor of the current mirror

oscillates between ground and V_{ref}. Consequently, the drain source voltage of transistor M13 is changing between V_{DD} and $V_{\mathrm{DD}} - V_{\mathrm{REF}}$. For this implementation, this is between 5 V and 1.5 V. In contrast, the drain voltage of transistor M11 is controlled to be at V_{REF}. Although a 1 µm technology is used, the effect of drain induced barrier lowering (DIBL) is occurring in this current mirror. Due to the high voltage at the drain, the depletion region of the drain moves towards the source resulting in a lower potential barrier. Electrons are injected to the channel more easily which can be regarded as a decrease of the threshold voltage [102].

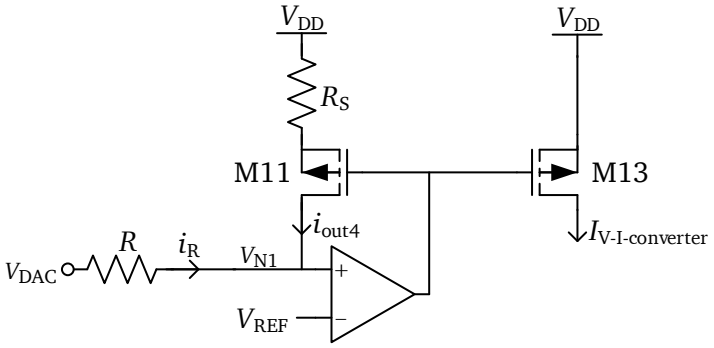


Figure 3.35.: Block diagram of the current mirror to drive the capacitance of the RC-oscillator. The regulation circuit of the voltage-to-current mirror is represented as an amplifier.

The DIBL effect results in a non-linear output current of the current mirror. This effect can be reduced by the help of a resistance at the source of the input transistor. Since both transistors work in saturation, the drain source current I_{DS} of the transistors, neglecting channel length modulation, is given by

$$I_{\mathrm{DS}} = \frac{K_{\mathrm{p}}}{2} (V_{\mathrm{GS}} - V_{\mathrm{TP}})^2 \tag{3.19}$$

with K_{p} being the gain factor of the PMOS transistor, V_{GS} being the gate-source voltage and V_{TP} being the threshold voltage of the PMOS transistor. If the threshold voltage of the output transistor M13 decreases, the output current increases. Due to the power of two, the output current $I_{\mathrm{V-I-converter}}$ curve is quadratic-shaped and is therefore more significant for higher current. To compensate this, the V_{GS} of the input transistor can be reduced which is done by a resistance at the source of the PMOS transistor.

The saturation voltage $V_{\mathrm{DS,sat13}}$ of the output transistor can be calculated by

$$V_{\mathrm{DS,sat13}} = V_{\mathrm{GS13}} - V_{\mathrm{TP13}} = V_{\mathrm{G11}} - V_{\mathrm{TP13}}. \tag{3.20}$$

The threshold voltage is reduced by ΔV_{TP}

$$V_{\mathrm{TP13}} = V_{\mathrm{TP11}} - \Delta V_{\mathrm{TP}} \tag{3.21}$$

due to the DIBL effect. The gate voltage of transistor M11 equals M13 and can be calculated by

$$V_{\mathrm{G11}} = V_{\mathrm{DS,sat11}} + R_{\mathrm{S}} i_{\mathrm{out4}} + V_{\mathrm{TP11}}. \tag{3.22}$$

According to Equation 3.19, the drain source saturation voltage $V_{\mathrm{DS,sat11}}$ is given by

$$V_{\mathrm{DS,sat11}} = \sqrt{\frac{2 i_{\mathrm{out4}}}{K_{\mathrm{p}}}}. \tag{3.23}$$

By inserting Equation 3.20, Equation 3.21, Equation 3.22 and Equation 3.23 in Equation 3.19, the DC characteristic curve $I_{\mathrm{V-I-converter}}\left(i_{\mathrm{out4}}\right)$ is given by

$$I_{\mathrm{V-I-converter}}\left(i_{\mathrm{out4}}\right) = \frac{K_{\mathrm{p}}}{2} V_{\mathrm{DS,sat13}}^2 = \frac{K_{\mathrm{p}}}{2}\left(\sqrt{\frac{2i_{\mathrm{out4}}}{K_{\mathrm{p}}}} + R_{\mathrm{S}} i_{\mathrm{out4}} + \Delta V_{\mathrm{TP}}\right)^2. \tag{3.24}$$

For optimal matching of the output current to the input current, the slope of $I_{\mathrm{V-I-converter}}\left(i_{\mathrm{out4}}\right)$ has to be minimized.This can only be achieved for a defined operating point I_{OP}. Consequently, the second deviation of the characteristic curve has to be zero at that operating point

$$\frac{\partial^2 I_{\mathrm{V-I-converter}}}{\partial i_{\mathrm{out4}}^2} \stackrel{!}{=} 0\Big|_{i_{\mathrm{out4}}=I_{\mathrm{OP}}}. \tag{3.25}$$

The resulting source degeneration resistance R_{S} can be calculated by

$$R_{\mathrm{S}} = \frac{2\Delta V_{\mathrm{TP}}}{3I_{\mathrm{OP}} + \sqrt{I_{\mathrm{OP}}\left(9I_{\mathrm{OP}} + 8\sqrt{2I_{\mathrm{OP}}K_{\mathrm{P}}}\Delta V_{\mathrm{TP}}\right)}}. \tag{3.26}$$

It can be implemented with a MOS transistor, as shown in Figure 3.32, which, in general, suffers less from process specifications than resistors.

Figure 3.36 shows the simulation results of the output current with respect to the input current. The output current characteristic can be linearized with the source degeneration resistance at the input transistor of the current mirror.

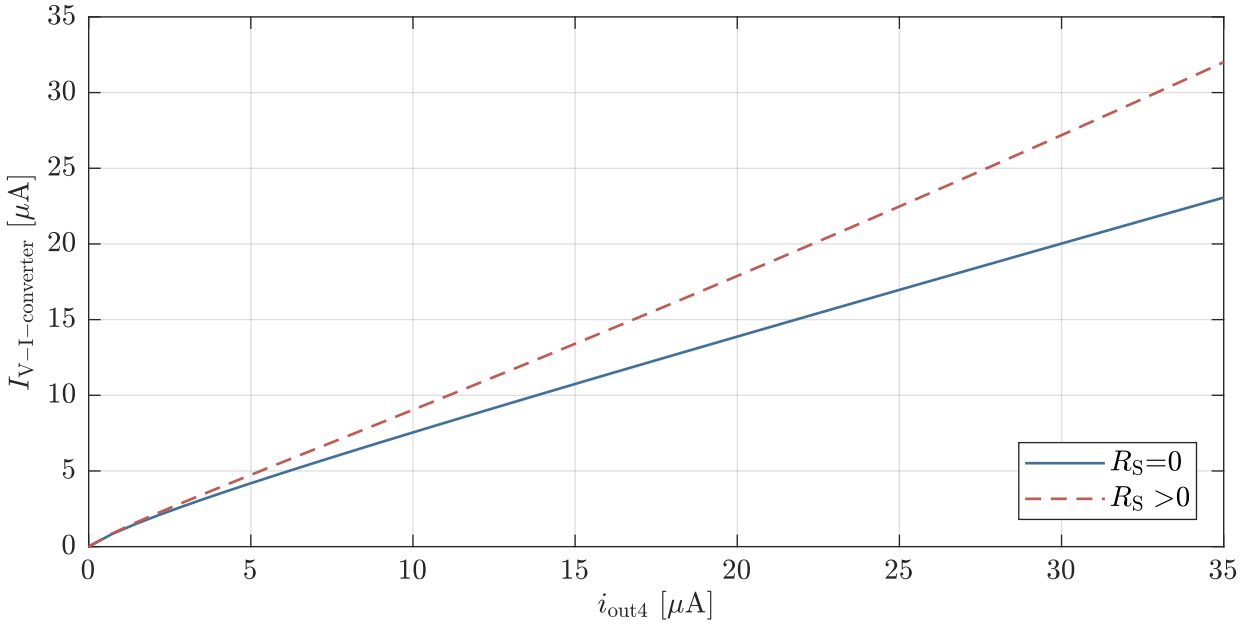
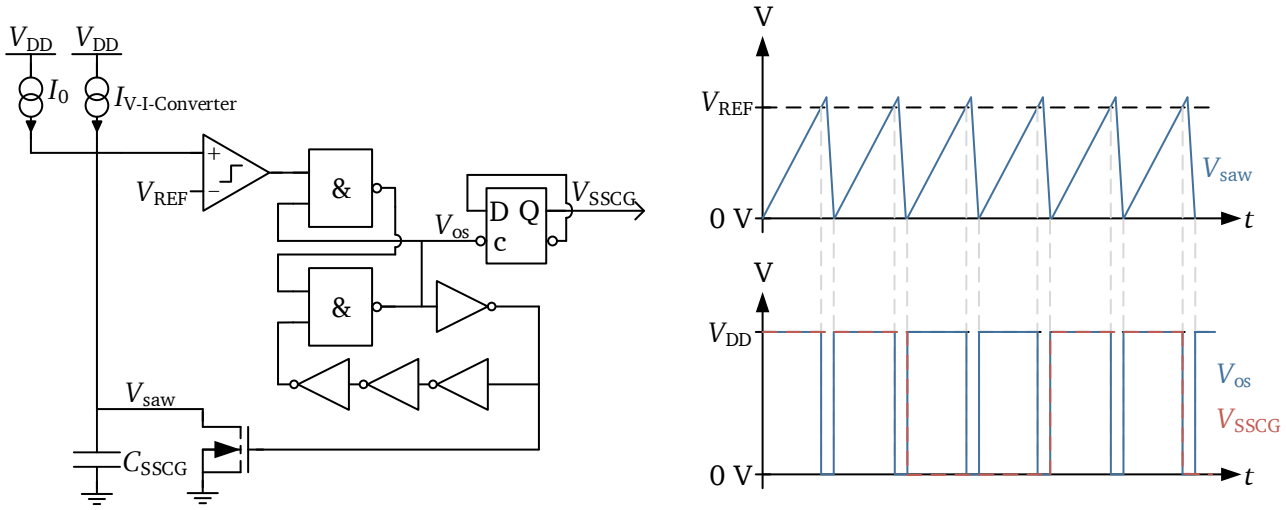


Figure 3.36.: Simulated input and output current of the current mirror. A source degeneration resistance R_{S} reduced the effect of DIBL due to high drain-source differences of the current mirror.

3.3.2.5 Implemented RC-oscillator Logic

The output current from the voltage-to-current converter $I_{\text{V–I–Converter}}$ charges a capacitor C_{SSCG} up to a voltage V_{REF}. Then, the comparator changes its output from zero to one as shown in Figure 3.37a. A subsequent RS-latch, implemented by two NAND gates, sets its output Q2 to zero, the oscillating voltage V_{OS} is 0 V. The charge on the capacitor C_{SSCG} is discharged by a parallel MOS transistor whose gate voltage increases to 5 V. The RS-latch is reset after a short time, defined by the four series connected inverters.

As shown in Figure 3.37b, the duty cycle of the oscillating voltage V_{OS} is very high. Since a duty cycle of 50 % is required for the spread spectrum technique, V_{OS} is connected to the clock input of a T-flip-flop which acts as a frequency divider. The output of the flip-flop can be buffered and connected to the sensor electrode.



(a) Schematic implementation of the logic within the SSCG.

(b) Characteristic waveforms of the SSCG logic.

Figure 3.37.: Implementation of the spread spectrum clock generator logic.

The output frequency of the spread spectrum clock generator f_{SSCG} is a function of the capacitance C_{SSCG}, its charging current, the reference voltage V_{REF} and the delay of the logic gates $t_{\text{delay,logic}}$

$$f_{\text{SSCG}} \approx \frac{1}{2\left(\frac{C_{\text{SSCG}} V_{\text{REF}}}{I_0 + I_{\text{V–I–converter}}}\right) + t_{\text{delay,logic}}}. \tag{3.27}$$

An additional current source with I_0 is implemented in parallel to the V-I converter to set the lower frequency as shown in the block diagram of the SSCG in Figure 3.24. The integrated logic occupies a chip area of 237.7 x 157.8 μm^2.

3.3.2.6 Implemented Tri-state Current Buffer

The output of the RC-oscillator logic V_{SSCG} is connected to a current buffer to be able to drive the capacitive sensor which was specified as up to 30 pF (see Table 3.2). The buffer has its own power supply and on-chip capacitor to be able to drive the high capacitive loads. As shown in Figure 3.38, its power supply is connected to the supply pad by a resistor of 14.2 Ω to reduce the ripple on the supply voltage. A capacitor of 68.06 pF stabilizes the internal power supply for the current buffer. The buffer has to be implemented as a tri-state buffer to disconnect the sensor excitation from the front electrode while the EL is lighted for the proposed multiplexing scheme. To be able to drive the large off-chip capacitor with a minimum delay, the sizing of the inverter chain within the buffer is of high importance. According to [103, p.216ff], the number of stages N can be calculated to

$$N = \ln \frac{C_{\text{load}}}{C_{\text{in1}}} = 6.96 \tag{3.28}$$

with an input capacitance C_{in1} of 28.54 fF which was determined by simulations. The different stages should be sized with a factor of

$$A = \left[\frac{C_{\text{load}}}{C_{\text{in1}}} \right]^{1/N} = 2.71\,. \tag{3.29}$$

However, this solution requires a large chip area. As suggested by [103], the number of stages can be reduced with only minimal extra delay. Therefore, for the presented IC, a solution with four stages and an area increase of 16 was implemented. Two inverter chains were implemented for the PMOS and for the NMOS output transistor, respectively, as shown in Figure 3.38. Since digital pads have an internal buffer which limit the output current, the output of the buffer is connected to an analog pad.

Post-layout simulations revealed a maximum delay of 7.74 ns for the worst speed corner. The current buffer has a total chip size of 519.30 x 486.20 μm^2 including the internal capacitor. Its power consumption for the worst case corner in post-layout simulations is 80.45 mW for an input signal of 8 MHz.

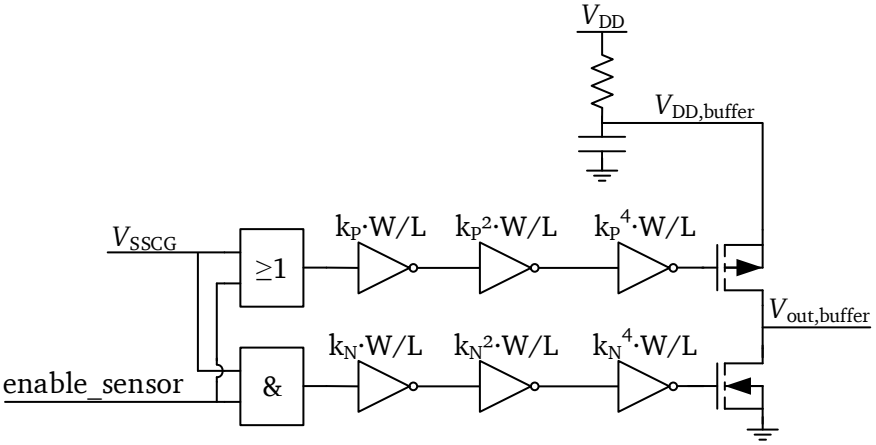


Figure 3.38.: Schematic of the implemented tri-state current buffer to drive a load of 30 pF.

3.4 Implemented High Voltage Integrated Circuits

The ultra high voltage pulse generator, described in subsection 3.2.2, and the spread spectrum clock generator, described in subsection 3.3.2, were designed and fabricated on a single IC in a 1 µm BCD SOI technology for voltages up to 650 V. The technology offers, inter alia, low, medium and high voltage NMOS and PMOS transistors, a variety of diodes for high and low voltages as well as high voltage capacitors in a three metal layer process. The SOI wafer is an n-doped wafer with a thick buried oxide of approximately 2 µm.

Two versions of the system-on-chip for the EL driver and the capacitive sensor excitation described in section 3.1 have been designed. Figure 3.39 shows the microphotograph of the first fully integrated SoC. The overall chip size is 6.570 x 5.865 mm^2. It includes a spread spectrum clock generator, a fully integrated dual NMOS inverter output stage including gate drivers, return-to-zero circuitry from the positive and the negative supply voltage as well as power transistors for positive and negative high voltage generation by boost and buck-boost converters, respectively [17].

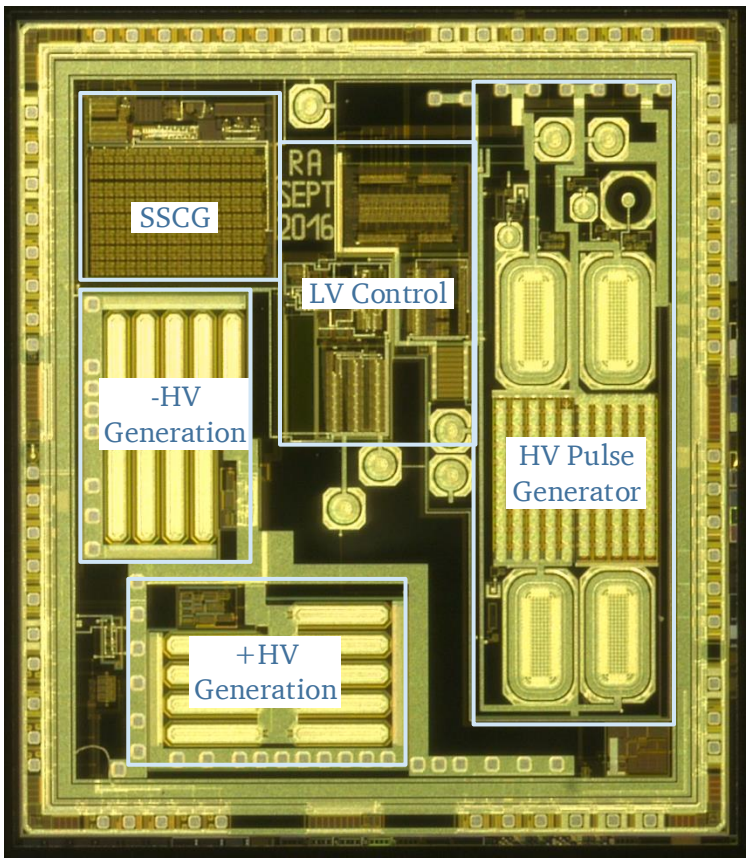
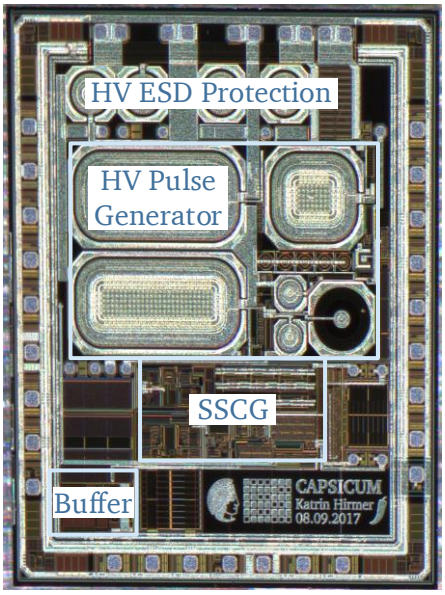
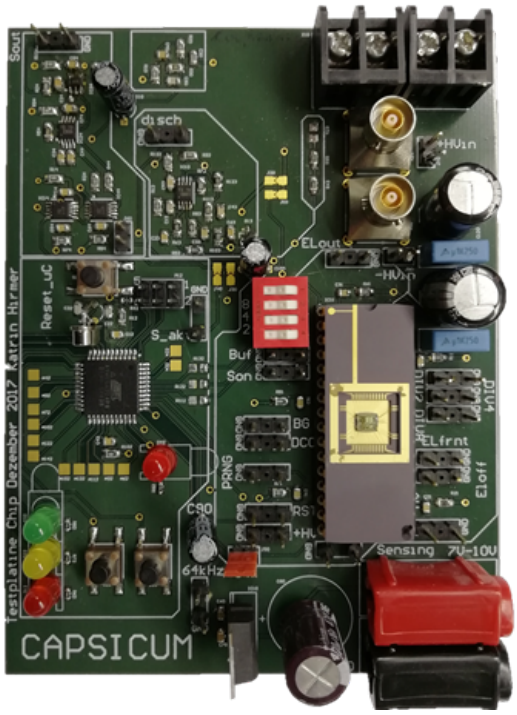


Figure 3.39.: Microphotograph of the first version of the fabricated SoC with spread spectrum clock generator, HV pulse generator and power transistors for the HV generation by boost and buck-boost converters.

For the sake of compactness, high current consuming components were taken off chip for the second implementation. The on-components were reduced to the fully integrated high voltage pulse generator and the spread spectrum clock generator. Figure 3.40a shows a microphotograph of the second version of the SoC. Its overall chip size is 2.910 x 3.435 mm^2. All measurements within this thesis were performed with this second edition of the SoC.



(a) Microphotograph of the SoC.



(b) PCB for measurements of the SoC.

Figure 3.40.: Experimental setup of the implemented SoC. The code name CAPSICUM is the abbreviation of "**Cap**acitive **S**ensing **I**llumination **C**hip for **U**sage in **M**otor Vehicle".

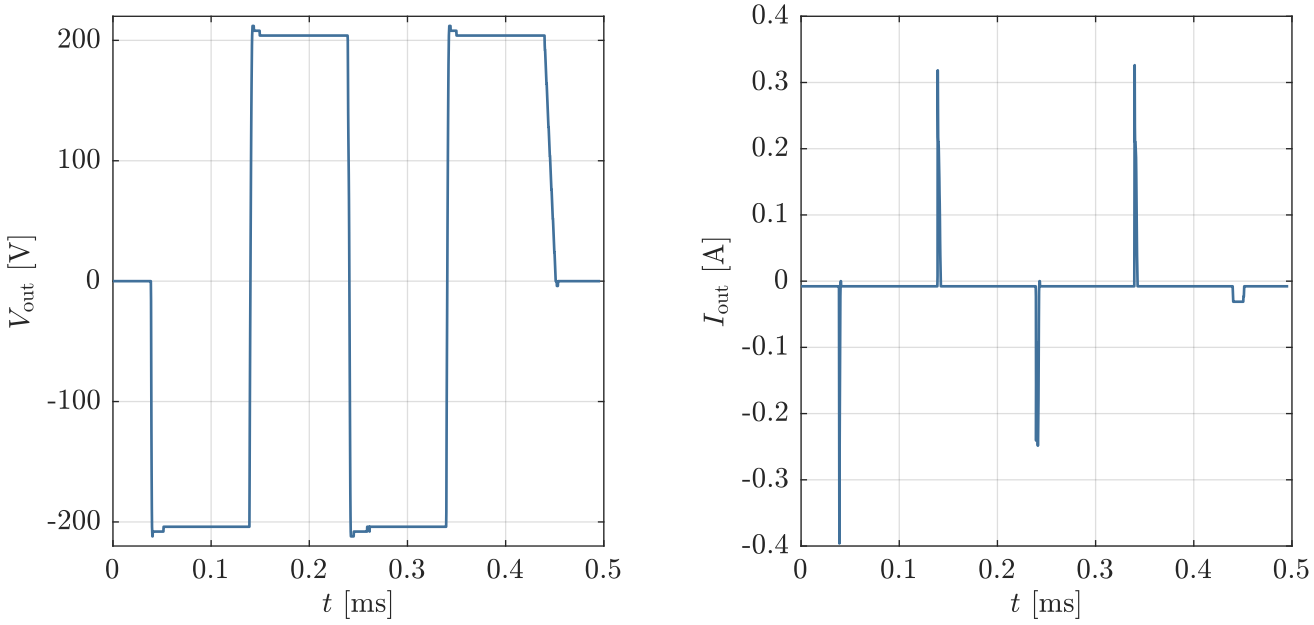
The different building blocks have separate supply voltage connections, each connected to an external 5 V power supply as previously shown in the block diagram of the SoC in Figure 3.6. The high voltage inverter of subsection 3.2.2 has a low supply voltage V_{DDHV} for the short circuit protection and the control of the gate drivers. The spread spectrum clock generator has two separate supply voltages. The analog parts such as voltage reference and voltage-to-current converter, described in subsubsection 3.3.2.1 and subsubsection 3.3.2.4, respectively, are connected to V_{DDa}. All digital components as well as the DAC are connected to a digital supply voltage V_{DDd}. The current buffer for driving the capacitive sensor, explained in subsubsection 3.3.2.6, is supplied by $V_{\mathrm{DD,Buffer}}$ due to the high power consumption of the buffer.

3.4.1 Characteristics of the Fabricated Inverter

The inverter including gate driver, presented in subsection 3.2.2, occupies an area of 2.61 x 1.31 mm^2. The majority of the chip area is occupied by the HV output DMOS transistors DM1, DM2 and DM3 since they have to deliver high output currents for the capacitive load. ESD protection for the high voltage inputs and outputs is also area consuming. The spread spectrum clock generator presented in subsection 3.3.2 occupies an area of 1.470 x 0.645 mm^2. It is positioned as close as possible to the inverter to force influences.

The stack of two wafers in thick SOI leads to an increased height of the IC. The overall height of the implemented HVIC was measured to 740 µm. Due to the thickness, modern package types such as quad-flat no-leads (QFN) packages cannot hold the IC which is why it was bonded into a dual-in-line package with 32 pins (DIL32). A printed circuit board (PCB) was designed to deliver the appropriate input signals for the purposes of research as shown in Figure 3.40b.

To ensure sufficient lifetime of the dies, measurements were only performed up to ±200 V. Figure 3.41a shows the measured output signal of the inverter which proves that it is able to drive capacitive loads with up to ±200 V at 5 kHz. The voltage was measured with a high voltage probe of type "TT-HV 250" from TESTEC Elektronik GmbH with an attenuation ratio of 100:1 [104]. It can be seen that all three states, positive high voltage supply, negative high voltage supply and ground, can be attained. The related output current was measured with a differential probe across a resistor of 10.3 Ω of type "TT-SI 9001" from TESTEC Elektronik GmbH [105]. An attenuation ratio of 10:1 was used. For an output load of 1 nF the peak output current was measured to -396.12 mA as shown in Figure 3.41b. The maximum output current for the fabricated inverter was measured for an output load of 10 nF. The measured 442.72 mA is 3.18 % smaller than the simulated peak current. Figure 3.41b also shows that the output current is limited for the return-to-zero transition resulting in a low slew rate of the output voltage.

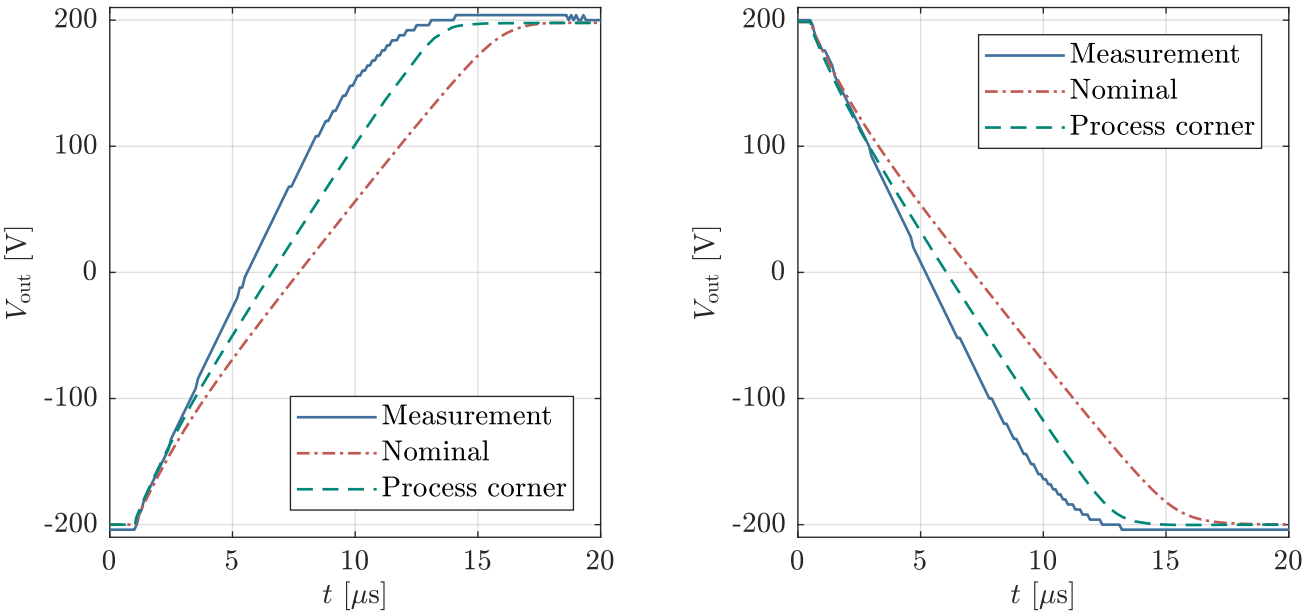


(a) Output voltage V_{out}.

(b) Output current I_{out}.

Figure 3.41.: Measured output characteristic of the fully integrated three-state inverter. Measurement was performed with an output load of 1 nF and a high voltage of ±200 V.

Figure 3.42 shows the measured and simulated rising and falling edge of the high voltage pulse generator output voltage for voltages up to $V_{\pm\text{HV}} = \pm 200\,\text{V}$ and an output load of $C_{\text{L}} = 10\,\text{nF}$. It can be seen that the slope of the measurement differs significantly from the nominal simulation. An analysis of the process control monitoring for the production run of this specific IC confirms the deviation. In fact, the production run for this IC had to be restarted due to poor quality of the measured device parameters. The evaluation of the fabricated devices revealed that the threshold voltages of the high and low voltage transistors are approximately 10 % lower than in the nominal simulation. For the resistances, the investigations revealed deviations of -8 % from the nominal value. Hence, the resistors can be better approximated by worst power corners. By simulating the process corner, the measurement can be predicted better.



(a) Rising edge.

(b) Falling edge.

Figure 3.42.: Comparison of measurement and simulation corners for the inverter output voltage V_{out} for $C_L = 10\,nF$ and $V_{\pm HV} = \pm 200\,V$.

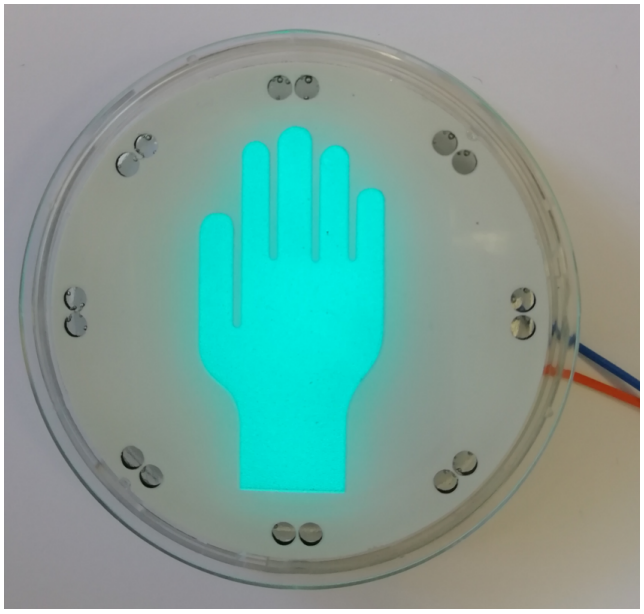
Figure 3.42 shows the falling and rising edges for the maximum output load of 10 nF and a voltage change of $400\,V_{PP}$ which result is a minimum slew rate and a maximum rising time. For this case, Table 3.5 lists the comparison of the measured and simulated slew rates. Slew rates of up to $39.35\,V\mu s^{-1}$ can be achieved for the maximum load which is about 21.30 % higher than the value simulated for the particular process corner.

Table 3.5.: Comparison of measured and simulated slew rate of the inverter output V_{out} for a high supply voltage of ±200 V and an output load of 10 nF.

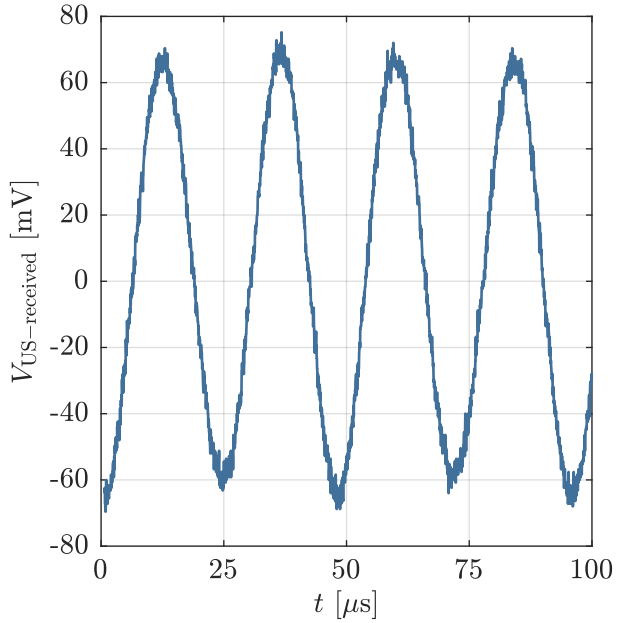
	Rising edge		Falling edge	
	measurement	simulation	measurement	simulation
$SR_{10-90}\,[V\mu s^{-1}]$	37.67	31.26	37.98	31.32

The minimum rising time was obtained for low magnitudes of the output voltage and a minimum capacitive load connected to the output. For 1 nF and an output voltage change of $100\,V_{PP}$ a maximum slew rate for the rising edge was measured to $99.56\,V\mu s^{-1}$. The corresponding rising time was measured to 1.00 µs. The slew rate for the falling edge is limited to $45.46\,V\mu s^{-1}$. The simulated value of $113.57\,V\mu s^{-1}$ is about 2.50 times higher than the measurement which can be traced back to production-related deviation and parasitic turn on of the high-side transistor.

The inverter was successfully connected to an electroluminescent device. The lighted EL is shown in Figure 3.43a. In addition, the inverter was connected to an ultrasound pulser of type MA40S4S [106] which represents a load of 2.55 pF. An output frequency of 40 kHz and supply voltages of $V_{\pm HV} = \pm 10\,V$ were achieved by the implemented inverter. The transmitted ultrasound signal was detected by a MA40S4R [106] as shown in Figure 3.43b. For the prove of concept the magnitude of the received signal is secondary since it is strongly dependent on the distance. Hence, the inverter can be used to drive capacitive loads.



(a) Fabricated inverter is driving a pad-printed electroluminescent device.



(b) Measured output signal of a received ultrasound wave.

Figure 3.43.: Prove of functionality of the inverter output for different applications.

3.4.2 Characteristics of the Fabricated Spread Spectrum Clock Generator

The spread spectrum clock generator described in subsection 3.3.2 occupies an area of 1463.5 x 639.0 µm^2. The data stream of the spread spectrum clock generator V_{SSCG} was recorded by a logic analyzer of type "Saleae Logic Pro 16" with a sampling rate of 500 MS/s. The frequency was extracted from the pulse period of the recorded data by a MATLAB based program. Figure 3.44 shows an excerpt from the measured output frequency over time. The frequency is hopped pseudo-randomly according to the PRN.

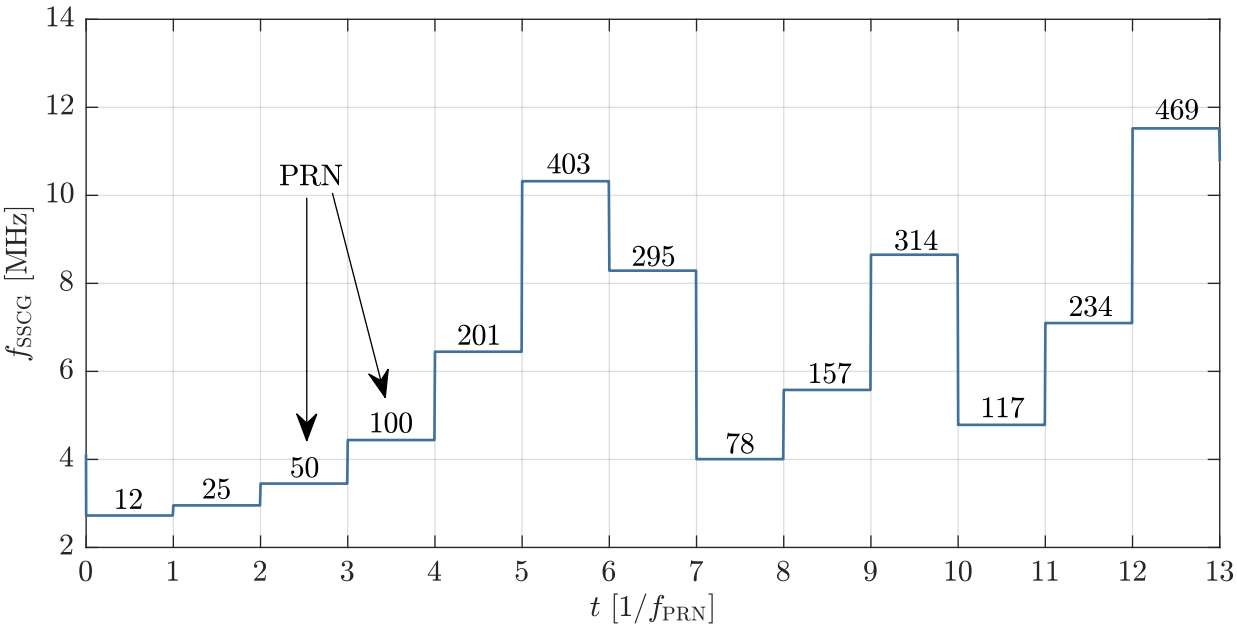


Figure 3.44.: Frequency hopping of the SSCG for different PRN with respect to time. The frequency of the PRN hopping f_{PRN} was 64 kHz which corresponds a time step of 15.63 µs.

Figure 3.45 shows the output frequency of the spread spectrum clock generator for all PRN. It shows a good linearity of the frequency over the complete bandwidth. However, it can be seen that the measured frequencies differ significantly from the nominal simulation. The measured frequencies are much higher than the simulated values for the nominal corner in post-layout simulation. Again, the spread spectrum clock frequency can be predicted more accurately by taking the process corner of the actual fabrication run into account. Although the measurement differs significantly from the nominal simulation, the specifications for the SSCG are satisfied, since the bandwidth with 10.14 MHz is higher than the minimum bandwidth of 4 MHz. Furthermore, the minimum frequency was specified to 125 kHz in Table 3.2 which is met by the implemented design.

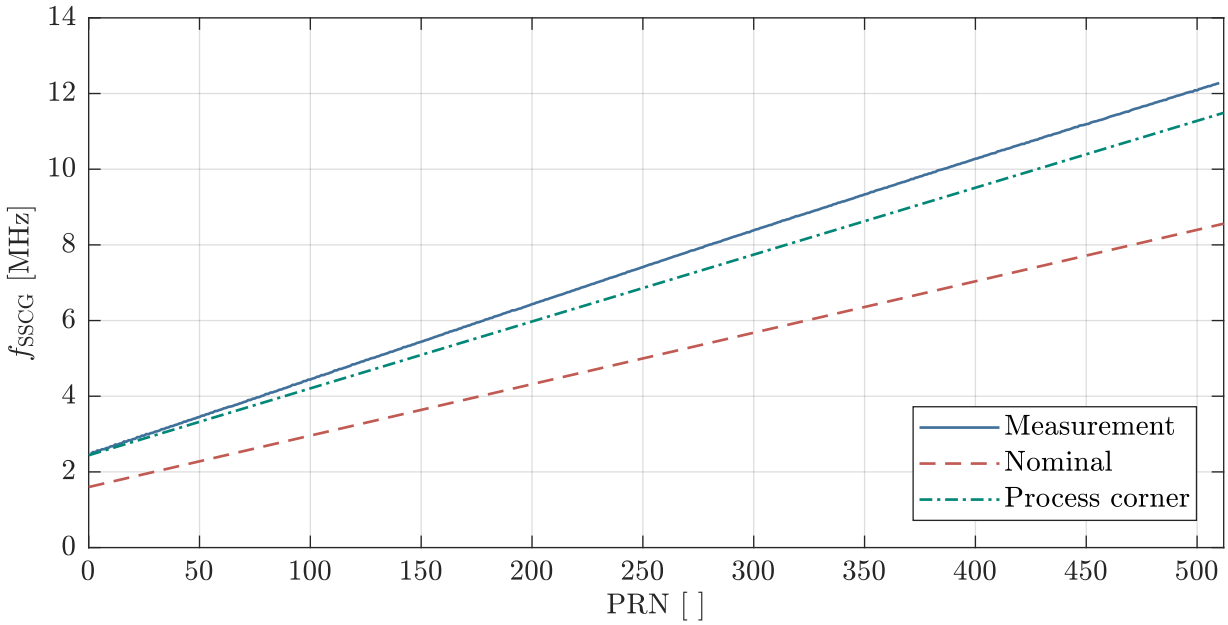


Figure 3.45.: Output frequency f_{SSCG} of the spread spectrum clock generator generator for the different pseudo-random numbers.

Figure 3.46 shows a detailed section of the output frequency for an MSB change of the DAC. A significant kink can be observed in the otherwise linear characteristic of the output frequency. This can be attributed to the faulty implementation of the DAC, as described in subsubsection 3.3.2.3. However, the differential non linearity error is less than one LSB.

The spectrum of the spread spectrum clock generator was measured with a spectrum analyzer HMS3010 from HAMEG® Instruments. The resolution bandwidth (RBW) was chosen smaller than the minimal frequency hop Δf of the SSCG which can be determined to

$$\Delta f_{\text{min}} = \frac{\Delta BW}{2^{\text{N}}} = \frac{4\,\text{MHz}}{512} = 7.81\,\text{kHz}. \tag{3.30}$$

Due to discrete setting options of the analyzer, the RBW was set to 300 Hz. The video bandwidth (VBW) was set to 1 kHz to reduce noise. The sweep time was set automatically by the spectrum analyzer to 827.77 s. Figure 3.47 shows that the SSCG generates main frequencies from 2.51 MHz to 12.65 MHz. The attenuation ΔP_{SSCG} compared to a non-spreaded device with a peak at 2.51 MHz is 33.17 dB.

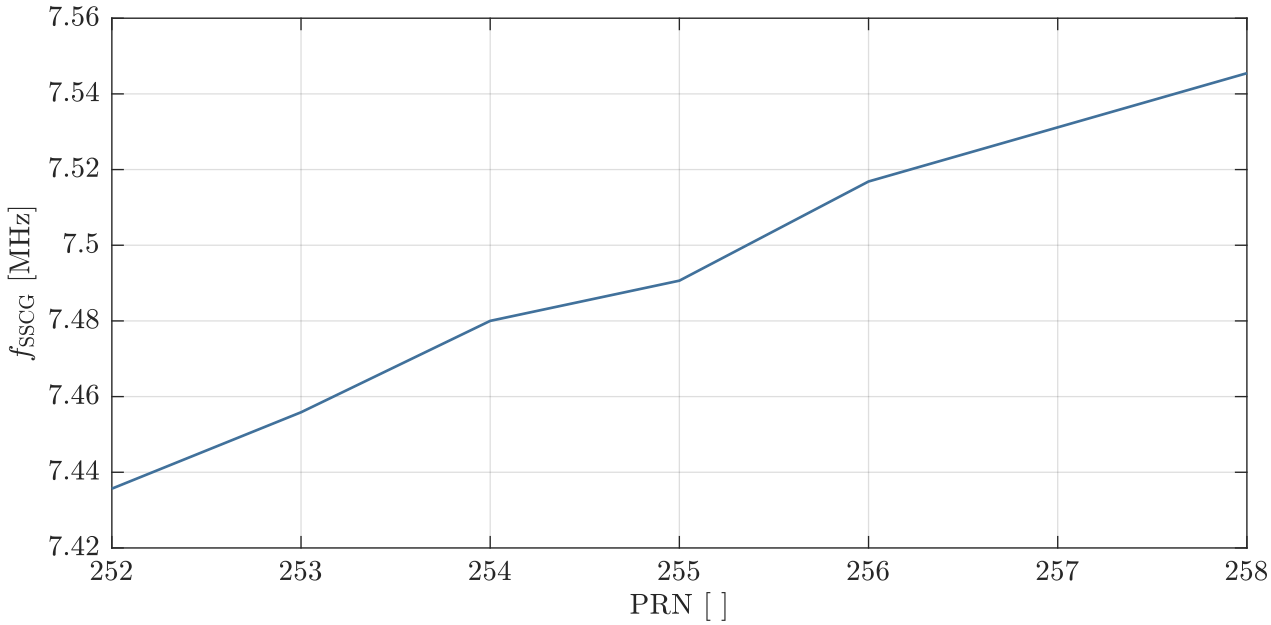


Figure 3.46.: Non-linear output frequency change of the spread spectrum clock generator for a change of the most significant bit of the DAC.

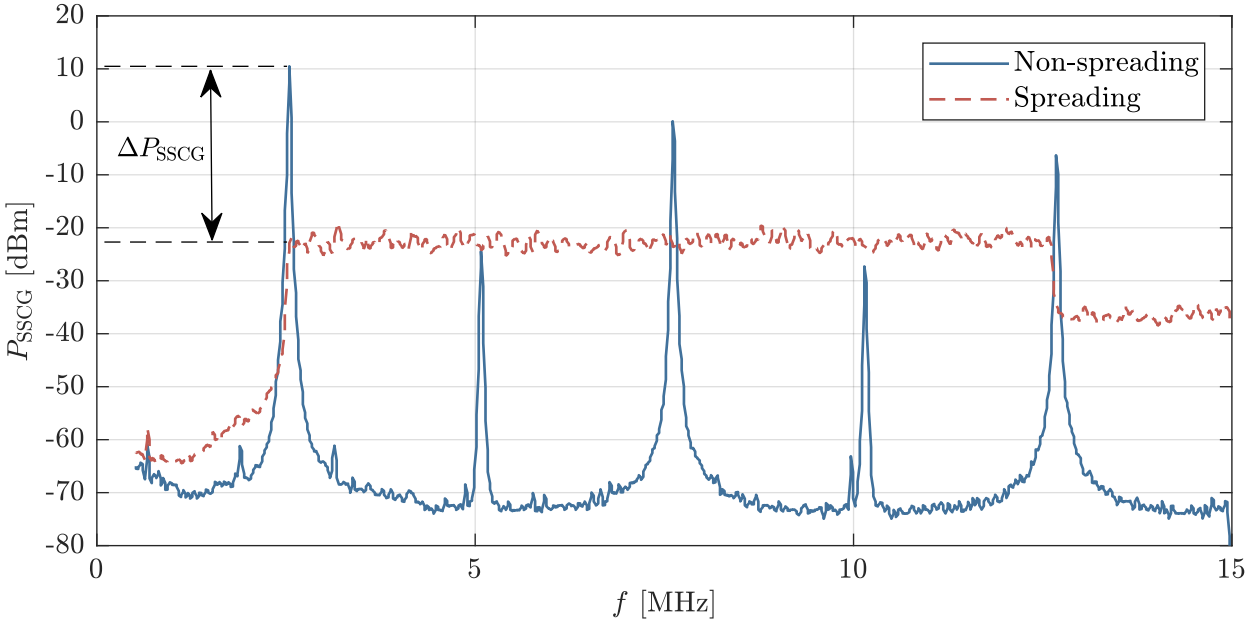


Figure 3.47.: Peak envelope of the measured spectrum of the spread spectrum clock generator with and without pseudo-random modulation.

3.5 Summary

To summarize, a high voltage integrated circuit including an ultra high voltage pulse generator and a low voltage spread spectrum clock generator were designed and fabricated in a 1 µm BCD SOI technology. It is able to drive an electroluminescent device which represents a capacitive load of up to 10 nF for the high voltage inverter. The inverter is fully implemented as a three-state inverter which can deliver output voltages of up to ±300 V with frequencies up to 5 kHz on a single-ended output. A return-to-zero circuit can remove any charge on the load capacitor before the sensor starts its task. The capacitive sensor is based on a spread spectrum technique which on the one hand allows the operation in harsh environments and on the other hand is conform with EMI standards for radiated power. The SSCG has a resolution of 9 bit with a minimum required bandwidth of 4 MHz.

Two versions of the SoCs were fabricated. The first version has a chip size of 6.570 x 5.865 mm^2 and includes a high voltage pulse generator, transistors for the high voltage generation, logic for the proposed multiplexing scheme and a spread spectrum clock generator. For the sake of compactness, a second IC with external high voltage generation and logic was fabricated with an overall chip size of 2.910 x 3.435 mm^2. Measurements confirm the functionality of the high voltage as well as of the low voltage building blocks. By taking the process corner of the actual run into account, the output voltage of the inverter as well as the frequencies of the SSCG for different pseudo-random numbers can be predicted well by simulations.

Measurements of the inverter revealed a maximum output current of 442.72 mA which differs from simulation by only -3.18 % for post-layout simulation with the process corner of the actual run. A maximum slew rate of 99.56 $V\mu s^{-1}$ was measured for a rising edge of the inverter. The inverter was connected to an electroluminescent panel and an ultrasound transmitter. Both applications could be operated successfully with the implemented inverter.

The spread spectrum clock generator has a linear output characteristic of the measured output frequency f_{SSCG} over the complete range of the pseudo-random number generator. Measurements show a bandwidth of 10.14 MHz with a minimum frequency of 2.51 MHz. The attenuation ΔP_{SSCG} compared to a non-spreaded device with a peak at 2.51 MHz is 33.17 dB.

In summary, the second version of the fabricated high voltage ICs contains building blocks with different high and low voltage components. The functionality of the high voltage as well as of the low voltage circuitry has been proven individually. For the proposed time multiplexing scheme of the presented application, electrical interferences are not expected since the components are not operated at the same time. However, for future extensions, the simultaneous use of the high voltage pulse generator and the mixed-signal designs is aimed at. Interferences of the low voltage circuitry due to high voltage pulses will be investigated in the following chapter. The second fabricated SoC serves as research object for practical measurements.

4 Interferences of Ultra High Voltage Pulse Generators on Low Voltage Circuitry

In chapter 3, a system-on-chip with an ultra high voltage pulse generator and a low voltage spread spectrum clock generator has been presented. Measurement results prove the functionality of the high voltage as well as the low voltage circuitry independently. However, interferences are observed for simultaneous use of the components of different voltage domains. Figure 4.1 shows that the output frequency of the implemented spread spectrum clock generator f_{SSCG} is changing with every edge of the high voltage pulse generator. This chapter aims at explaining and modeling these interferences.

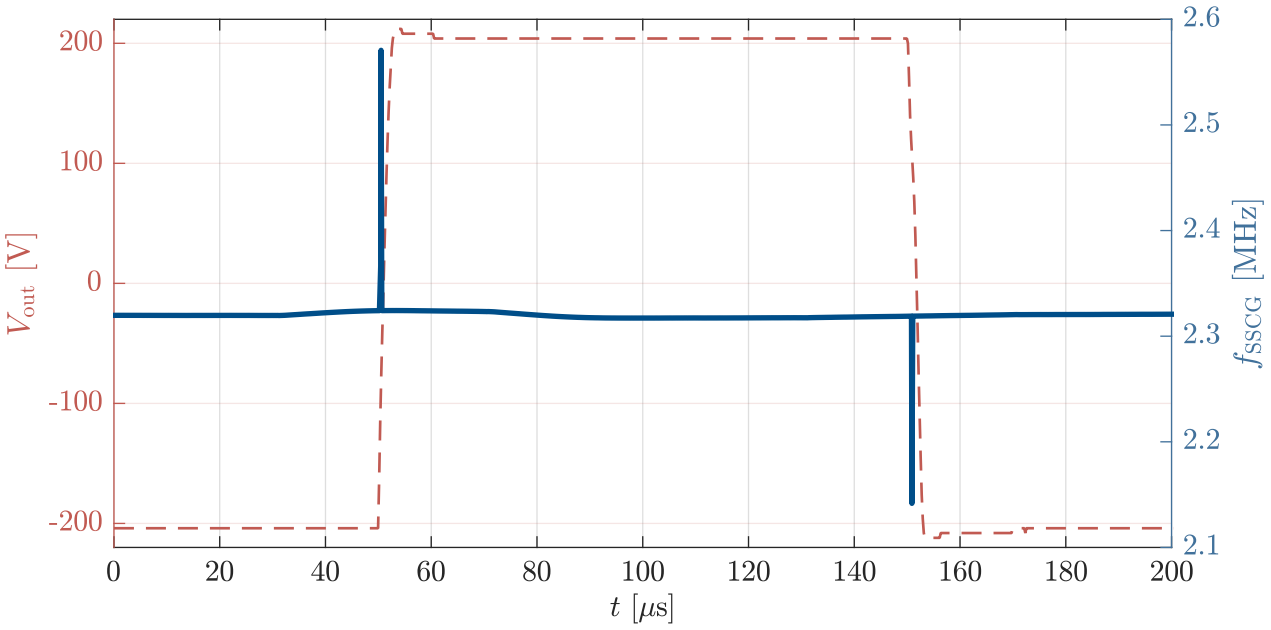


Figure 4.1.: Measured influences on the output frequency of a spread spectrum clock generator f_{SSCG} by a monolithically integrated high voltage pulse generator.

In general, interferences due to electrical coupling can be divided based on their physical effect. Four different effects can be distinguished as shown in Figure 4.2 [107]. Field-bound coupling by radiation is only relevant for far field applications and cannot occur in integrated circuits due to the limited dimensions of the IC. However, near-field coupling as well as conductive coupling can cause interferences within different components of the IC. Therefore, galvanic coupling, capacitive coupling and inductive coupling have to be addressed for SoCs with ultra high voltage pulse generators and sensitive low voltage circuitry.

Galvanic coupling can occur if the different components share the same potential such as, for example, the supply rails. To prevent galvanic coupling on the IC, the different components have to be supplied with different supply voltages over separate pads. However, any shared impedance can cause conductive coupling within an IC and has to be avoided.

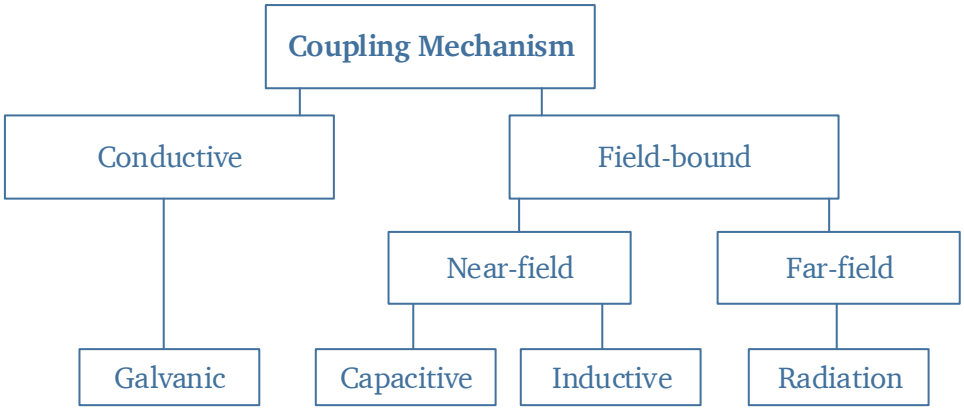


Figure 4.2.: General overview of coupling mechanisms in electrical systems (adapted from [108]).

In capacitive coupling, the energy is transmitted via the electric field. It is dependent on the geometries of the two conductors, their distance from each other as well as the permittivity of the material in between. In addition, it is also dependent on the slew rate of the interfering signal [107].

Inductive coupling transmits energy through the magnetic field. Again, the strength of the coupling depends on the geometries of the conductors on the IC. Parallel conductors that are very close to each other and signals with high current changes have high magnetic couplings [107].

Inductive and capacitive field-bound coupling can cause disturbances and failures within different circuit building blocks. Layout extraction methods are established in the IC design flow as explained in section 2.3. They can cover some of these coupling aspects such as coupling between and resistances of metal and polysilicon wires within the IC. However, substrate coupling, which is a big issue for many IC designers, is not always covered by conventional EDA tools. This is why it has been investigated with respect to mixed-signal ICs [109, 110], radio-frequency [111, 112, 113] and high voltage [114, 45, 115] applications. In the past, efforts have been made to integrate the effect of the coupling via the substrate into the IC design flow [116, 117]. However, it is still a big issue for HVICs [45] and has to be addressed by the designer during the design phase.

For high voltage integrated circuits fabricated in a bulk CMOS process, the high voltage pulses can introduce charge into the bulk material which represents a common node for high and low voltage devices [36]. This charge can be a base current for parasitic bipolar junction transistors which are present due to p-n-junction from the mostly p-substrate to any n-well of the circuit implementation. As a consequence, the substrate suffers from a voltage shift which can disturb surrounding circuitry or even cause a latch up in the HVIC [45].

In deep trench isolation and silicon-on-insulator technologies, the substrates of different circuit components are separated by vertical and for SOI additionally by horizontal isolating material such as silicon oxide (SiO_2). Hence, parasitic BJTs are not dominating in SOI HVICs. However, the high voltage switching can cause capacitive coupling to the handle wafer due to the buried oxide [20]. In this case, the handle wafer represents a common node which enables galvanic coupling. Consequently, charge can capacitively couple across the handle wafer and the buried oxide to low voltage circuitry on the IC. These effects are not covered by parasitic extraction within the standard design flow and hence not covered by post-layout SPICE simulations.

Raskin et al. have investigated the substrate coupling effects in SOI ICs in [20]. They found that a significant part of the coupling current in SOI flows in the active wafer substrate close to the buried oxide.

Therefore, Raskin et al. as well as others suggest the introduction of a highly doped layer on top of the buried oxide which is connected to an appropriate DC voltage such as ground or V_{DD} for p-substrate and n-substrate, respectively [20, 118]. Hence, any switching noise on the handle wafer in SOI ICs, especially for high voltages, is capacitive shielded by the highly doped region above the BOX.

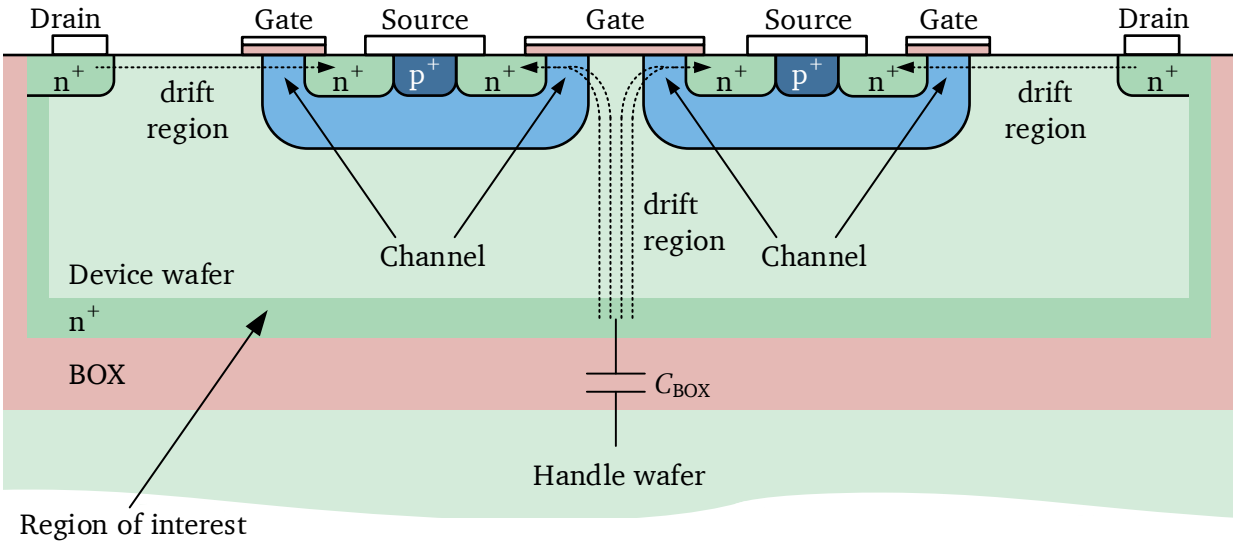


Figure 4.3.: Structure of an n-channel quasi-vertical DMOS transistor in an SOI technology (adapted from [13]). The n^+-drain-region close to the buried oxide is coupling into the substrate handle wafer.

By implication, this highly doped region above the BOX can introduce high parasitic currents into the handle wafer if it is connected to a high voltage switching signal. As shown in Figure 4.3, quasi-vertical n-channel DMOS transistors, as in the case of the fabricated HVIC, have their drain connected to the particular region of interest. If the drain contact of these devices is connected to a switching voltage, high coupling to the handle wafer is expected.

As described in subsection 3.2.2, the implementation of ultra high voltage pulse generators without using n-channel DMOS transistors is not feasible due to the large chip area of HV PMOS transistors. The output stage of dual NMOS inverter circuits is shown schematically in Figure 4.4. The drain of the low-side quasi-vertical DMOS transistor DM2 is connected to the switching high voltage output. As a result, capacitive coupling to the handle wafer can be expected due to the structure of the DMOS transistors shown in Figure 4.3.

For low voltage tubs within an n-substrate IC, the n^+-region above the BOX is mostly connected to the highest potential to keep the pn-junctions within the active tub reverse biased. Consequently, signals from the high voltage devices of the IC can couple capacitively to the handle wafer and from there in turn capacitively to the bulk of the active tub, which is mostly connected to the supply voltage V_{DD} of the low voltage circuitry.

For the application presented in section 3.1 and the implemented HVICs presented in section 3.4, substrate coupling can be expected due to the low-side NMOS transistor of the fully integrated three-state high voltage pulse generator. Therefore, the effects of substrate coupling in SOI HVICs will be discussed in the following subsections. Parts of this chapter have already been published in [47] and [49].

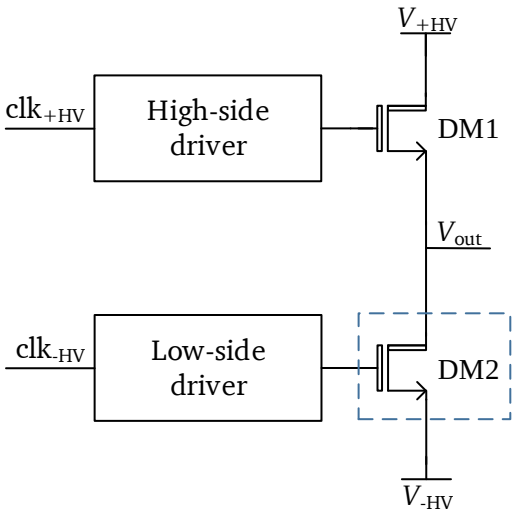


Figure 4.4.: Schematic representation of a dual NMOS output stage. The drain of the low-side quasi-vertical DMOS transistor DM2 is connected to the switching high voltage output.

4.1 Electrical Equivalent Circuit of the Substrate Coupling in Thick SOI

In thick SOI processes, capacitive coupling between high voltage and low voltage components can happen both through the substrate and through the trenches. Figure 4.5 shows the equivalent circuit of the substrate network through the buried oxide and the handle wafer as well as the trench capacitance C_{T12}. Terminals one and two are the connections to independent active silicon tubs (e.g. high voltage and low voltage tubs), terminal 3 is the backside connection of the silicon handle wafer. It is usually conductively glued to the bottom of the package. The gold plating of the packaging is highly conductive which is why the handle wafer contact can be regarded as a short and hence as one contact. The silicon handle wafer can be regarded as a resistive and a capacitive network. The values for R_{ij} and C_{ij} can be calculated using the physical parameters of the handle wafer material such as the doping concentration and related relative permittivity and conductivity.

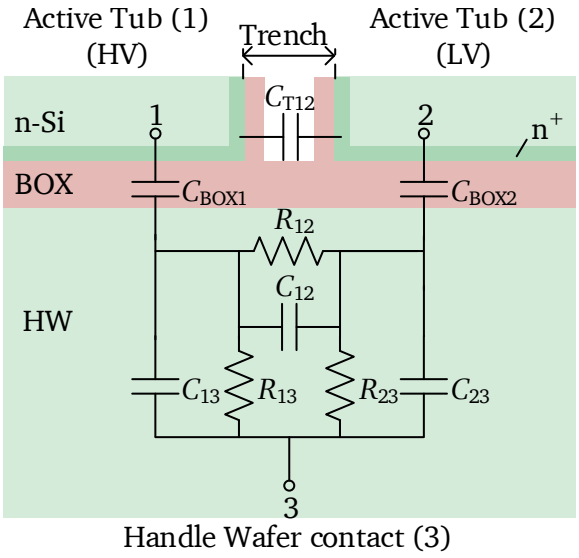


Figure 4.5.: Equivalent circuit of the handle wafer substrate (adapted from [20]).

In Figure 4.5, it can be seen that coupling between two adjacent tubs can happen in two different ways. First, charge can be capacitively coupled through the trench by C_{T12}. Second, it can couple from one tub to the handle wafer and then through the buried oxide to the second tub. The coupling through the trench by C_{T12} can be neglected, if it is much smaller than the series connection of C_{BOX1} and C_{BOX2}

$$C_{T12} << C_{BOX} = \frac{C_{BOX1} C_{BOX2}}{C_{BOX1} + C_{BOX2}} \approx C_{BOX2}, \tag{4.1}$$

which is approximately equal to C_{BOX2} if it is assumed that the area of the low voltage components (tub 2) is much smaller than the high voltage components and the voltage drop across R_{12} can be neglected. C_{BOX2} can also be regarded as a parallel plate capacitor and represented as

$$C_{BOX2} = \frac{\epsilon_0 \epsilon_r w_{Device} l_{Device}}{d_{BOX}} \tag{4.2}$$

with the thickness of the buried oxide d_{BOX} and its relative permittivity ϵ_r. The area of the tub is given by its width w_{Device} and its length l_{Device}.

The trench capacitance can be regarded as a series connection of two capacitances since the filling between the isolating trench oxide (TOX) usually consist of polysilicon which is highly conductive and hence can be regarded as a short. The overall capacitance between two adjacent tubs C_{T12} can be calculated with a parallel plate approach by

$$C_{T12} = \frac{\epsilon_0 \epsilon_r w_{Device} h_{Device}}{2 d_{TOX}}. \tag{4.3}$$

The physical dimensions such as thickness d_{TOX} and relative permittivity ϵ_r of the trench oxide as well as width w_{Device} of the tub and height h_{Device} of the active wafer are required to calculate the coupling capacitance.

Since the trench oxide and the buried oxide consist of silicon dioxide, their relative permittivity ϵ_r is equal. By inserting Equation 4.2 and Equation 4.3 in Equation 4.1, it can be concluded that the coupling through the trench capacitance can be neglected if

$$h_{Device} << 2 l_{Device} \frac{d_{TOX}}{d_{BOX}}. \tag{4.4}$$

For thick SOI processes, the trench oxide is usually much thinner than the buried oxide [119]. So for worst case considerations, they can be regarded as equal in size , resulting in

$$h_{Device} << 2 l_{Device}. \tag{4.5}$$

For several trenches N between the high voltage and low voltage tubs, C_{T12} can be neglected if

$$l_{Device} >> \frac{h_{Device}}{2N}. \tag{4.6}$$

For thick SOI technologies with minimum structure size of 1 µm and a device wafer height of approximately 55 µm, the length of the tub will usually be larger than half of h_{Device} and hence C_{T12} can be neglected. Therefore, the coupling across the handle wafer substrate has a more significant impact and is investigated in the following.

4.1.1 Analytic Equations of Parasitic Components for Hand Calculation

The substrate network in Figure 4.5 has been introduced with focus on higher frequencies [20] or on SOI technologies with thin buried oxides and high-resistive substrates which are optimized for RF rather than for HV [120]. For frequencies below

$$f << \frac{1}{2\pi\epsilon_0\epsilon_r\rho}, \tag{4.7}$$

with ϵ_r and ρ being the permittivity and the resistivity of the silicon handle wafer, the equivalent substrate network is dominated by the buried oxide capacitances $C_{BOX,i}$ and the resistive part of R_{12}, R_{13} and R_{23} since the impedance of the capacitance is much higher than the resistance of the handle wafer

$$Z_{C,ij} >> R_{ij}. \tag{4.8}$$

The parallel connection of R_{ij} and C_{ij} reduces to R_{ij} only. For lightly doped n-type silicon as for the handle wafer, a majority carrier concentration of phosphorous atoms N_D of $1.0{\cdot}10^{15}\,cm^{-3}$ ca be assumed [37]. From this, a resistivity of $0.04\,\Omega m$ can be calculated [121]. Consequently, a cutoff frequency f of 38.41 GHz can be calculated with Equation 4.7. For applications with lower frequencies, such as the maximum inverter frequency of 5 kHz and a maximum slew rate of $99.56\,V\mu s^{-1}$ for the application described in section 3.1, the capacitive behavior of the silicon handle wafer can be neglected.

For each tub, the capacitance between the tub and the handle wafer $C_{BOX,i}$, the resistance of the handle wafer R_{i3} and the resistance to other tubs R_{ij} have to be determined. The analytic equation for these parameters will be presented in the following. The capacitance for an active tub i to the handle wafer can be calculated as a parallel plate capacitor on the assumption of a homogeneous capacitance per area and it can be denoted as

$$C_{BOX,i} = \frac{\epsilon_0\epsilon_r A_i}{d_{BOX}} \tag{4.9}$$

with A_i being the area of the active tub as well as ϵ_r and d_{BOX} being the permittivity and the thickness of the buried oxide, respectively. The buried oxide is composed of silicon dioxide with $\epsilon_{r,BOX} = 3.9$ and a thickness of $d_{BOX} = 2\,\mu m$ for thick BOX SOI wafer [35].

Neglecting fringe effects within the thick handle wafer, the resistance of each tub to the bottom of the handle wafer can be approximated by

$$R_{i3} = \frac{\rho\, d_{HW}}{A_i}. \tag{4.10}$$

It increases with the resistivity ρ of the handle wafer material and decreases with the area of the active tub A_i.

The resistance R_{ij} between two active tubs i and j can be approximated by

$$R_{ij} = \frac{\rho\, d_{ij}}{\overline{b_{ij}} d_{HW}}. \tag{4.11}$$

The resistance increases with the distance between the centers of the device tubs d_{ij}. The area of the current path can be approximated by the thickness of the handle wafer d_{HW} and the mean of the width of the two tubs b_i and b_j, respectively, as follows:

$$\overline{b_{ij}} = \frac{b_i + b_j}{2}. \tag{4.12}$$

Heinle et al. showed that the approximation of the capacitance $C_{BOX,i}$ using the parallel plate approach is sufficient for low frequency applications [122]. This is only true if the area of the device tub is large enough and hence the fringing effects are negligible. Values for the fringing factors of the resistance are given in [20]. However, these values are semi-empirical and are optimized for higher frequencies. A second approach is to extract the resistance values by the help of three-dimensional (3D) field simulations. This is considered in the following section.

4.1.2 Extraction of Values for Parasitic Components by 3D Field Simulations

Technology Computer Aided Design tools can help simulate the electrical, mechanical, thermal and optical behavior of a system with the help of 3D field simulations. In this work, Sentaurus TCAD from Synopsys® is used to extract the exact values for the substrate network.

The coordinates for the electrodes are extracted from the layout of the HVIC described in section 3.4. Values for R_{i3} and C_{i3} can be extracted from AC simulations in Sentaurus Device within TCAD. For these simulations, a 1 µm thick gold plate is positioned at the bottom of the handle wafer to which the die is usually glued. Again, a majority carrier concentration of phosphorous atoms N_D of $1.0{\cdot}10^{15}$ cm^{-3} for the lightly doped handle wafer is assumed. The thickness of the handle wafer has a height of 570 µm. The simulations were performed at 5 kHz with frequency independent material modeling.

As expected, the simulated values for R_{i3} are smaller compared to the calculations described in subsection 4.1.1. This is due to the stray effects within the thick handle wafer. Fringing capacitances lead to an increase of C_{i3} compared to the calculated values. These effects increase with smaller areas of the tubs leading to significant discrepancies between simple hand calculations and TCAD simulations.

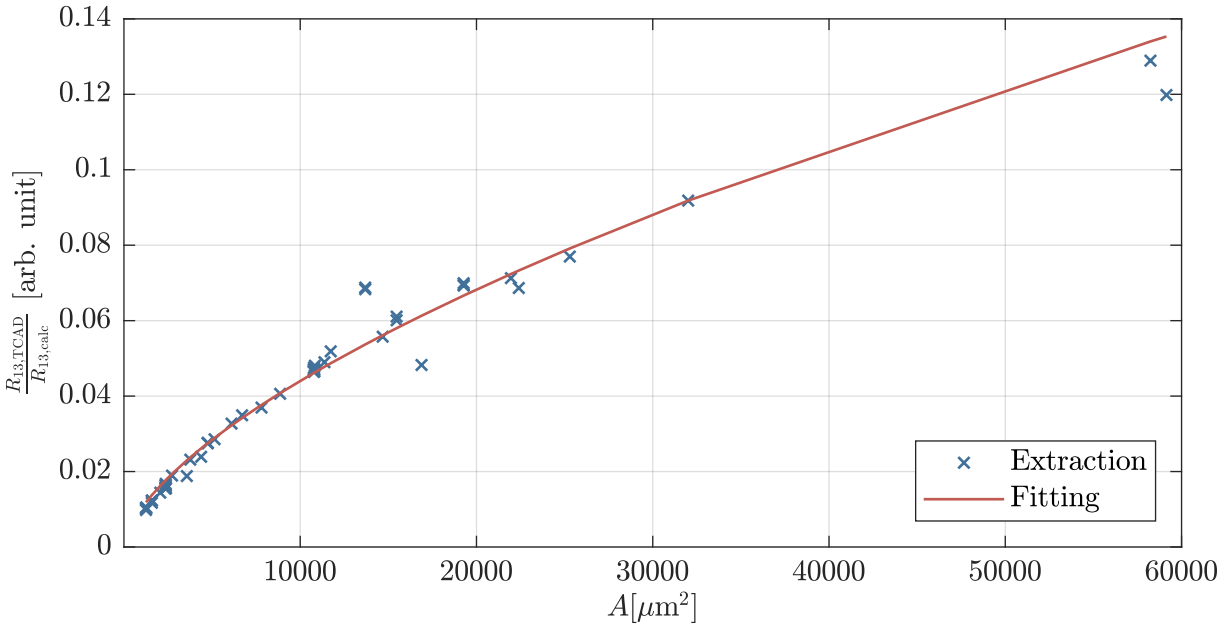


Figure 4.6.: Correction factor for the calculation of R_{13} with respect to the active area of the tub.

The extracted values for R_{i3} and C_{i3} are compared to the calculated values. Figure 4.6 shows the ratio of the value $R_{13,TCAD}$ obtained by TCAD simulations and the value $R_{13,calc}$ calculated by Equation 4.10. It can be seen that the factor increases with the active tub area A since fringing effects have a lower impact as the active tub size increases. Nevertheless, the absolute value of the ratio is very small, even for the area-consuming high voltage DMOS transistors. The values calculated with Equation 4.10 are thus significantly larger than those simulated with TCAD. The ratio of $R_{13,TCAD}$ and $R_{13,calc}$ can be fitted by a power equation with an R^2 accuracy of 0.99 by

$$\frac{R_{13,TCAD}}{R_{13,calc}} = a_{R13} \cdot A^{b_{R13}} \tag{4.13}$$

with $a_{R13} = 1.31 \cdot 10^{-4}\,\mu m^{-2}$ and $b_{R13} = 0.63$.

For higher frequency ranges, the approximation of C_{13} can be corrected for fringing capacitances within the handle wafer. Figure 4.7 shows the ratio of the value simulated with TCAD $C_{13,TCAD}$ by the calculated value $C_{13,calc}$

$$C_{13} = \frac{\epsilon_0 \epsilon_{r,Si} A_i}{d_{HW}}. \tag{4.14}$$

It can be seen that the deviation in correction factor for C_{13} decreases with increasing tub area. Again, the resulting values can be fitted by a power law with an R^2 accuracy of 0.99 by

$$\frac{C_{13,TCAD}}{C_{13,calc}} = a_{C13} \cdot A^{b_{C13}}. \tag{4.15}$$

with $a_{C13} = 1.54 \cdot 10^{4}\,\mu m^{-2}$ and $b_{C13} = -0.71$.

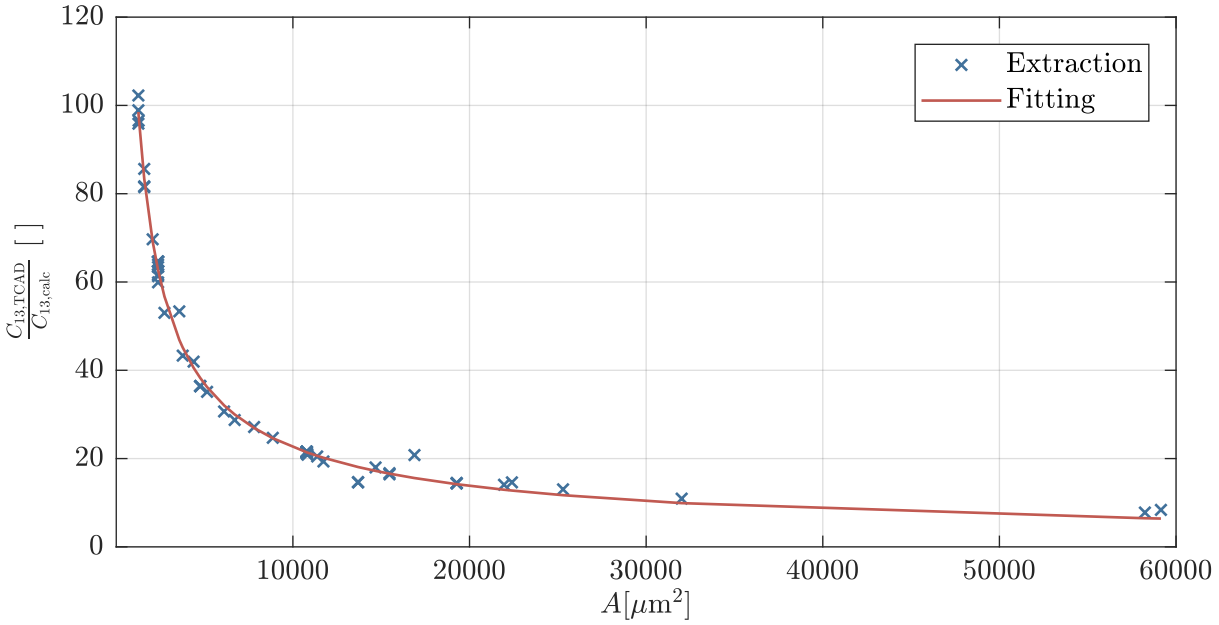


Figure 4.7.: Correction factor for the calculation of C_{13} with respect to the active area of the tub.

Figure 4.8 shows the ratio of the value simulated with TCAD $C_{\mathrm{BOX,TCAD}}$ by the calculated value $C_{\mathrm{BOX,calc}}$. The capacitance for the buried oxide C_{BOX} can also be fitted by a power law. However, the ratio of the value $C_{\mathrm{BOX,TCAD}}$ obtained by TCAD simulations and the calculated value $C_{\mathrm{BOX,calc}}$ of Equation 4.9 is more scattered with respect to the active tub area A. Hence, the accuracy is reduced compared to the fitting of C_{13} and R_{13}.

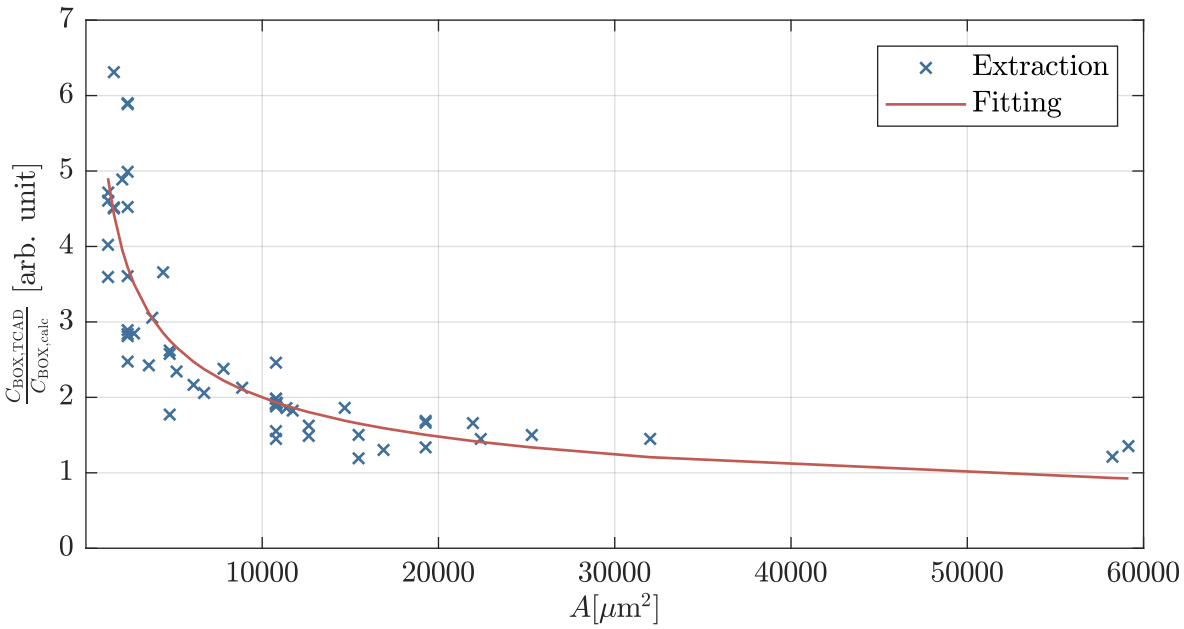


Figure 4.8.: Correction factor for the calculation of C_{BOX} with respect to the active area of the tub.

An R^2 fitting accuracy of 0.73 can be achieved by

$$\frac{C_{\mathrm{BOX,TCAD}}}{C_{\mathrm{BOX,calc}}} = a_{\mathrm{CBOX}} \cdot A^{b_{\mathrm{CBOX}}} \tag{4.16}$$

with $a_{\mathrm{CBOX}} = 107.30\,\mu\mathrm{m}^{-2}$ and $b_{\mathrm{CBOX}} = -0.43$. Due to the power law of the fitting, any deviation of the fitting to the TCAD simulated value has a significant impact and introduces an error for large layout areas. Therefore, high voltage DMOS transistors should be excluded from the correction. Due to the large area, the fringing capacitances are not very significant. Their values can be calculated with sufficient accuracy by Equation 4.10 and Equation 4.9.

The parameters R_{ij} and C_{ij} are functions of the areas of two tubs as well as of their distance. Their values cannot be improved over the entire range of areas and distances by using a single correction factor. This is why the approximation of R_{ij} is made by Equation 4.11, whereas C_{ij} is neglected for analytic calculations for low frequency operation. An accurate determination of the values can only be achieved by TCAD simulations.

4.2 Automated Extraction of the Substrate Network

The parasitic substrate network can be extracted from the IC layout. The Cadence® based scripting language SKILL® can be used to generate the substrate netlist automatically. The design flow is shown in Figure 4.9. The program code can be found in Appendix C.

In the first step, the layout can be reduced to focus on the influences of special nets or of sensitive parts i.e. high voltage switching inverter output on analog circuitry. The area and the distance of the active

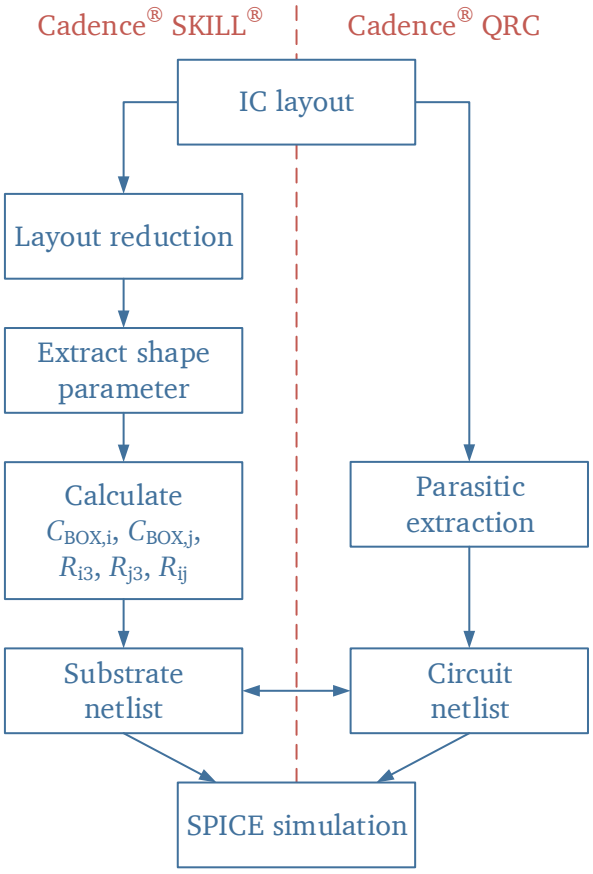


Figure 4.9.: Design flow of the parasitic substrate extraction.

tubs that are connected to the requested nodes can be extracted from the IC layout. These parameters can be used to approximate the value $C_{BOX,i}$, $C_{BOX,j}$ as well as the resistances R_{i3}, R_{j3} and R_{ij} by Equation 4.9, Equation 4.10 and Equation 4.11, respectively. The correction terms for $C_{BOX,i}$ of Equation 4.16 as well as for R_{i3} and R_{j3} of Equation 4.13 can be included in the calculation. For high frequency operation, the substrate parameters for C_{i3}, C_{j3} and C_{ij} can be included additionally. By connecting the substrate components to the related nets, a substrate netlist can be generated according to the substrate equivalent circuit shown in Figure 4.5. The net names of the connection to the tub nets should comply with the net names of the schematic implementation. This procedure simplifies the co-simulation with the actual circuit.

In addition to the substrate netlist, a netlist of the actual circuit within the IC layout can be obtained for post-layout simulations. It mostly includes parasitic resistors and capacitances and can be created with the help of tools integrated in the design flow, such as Cadence®Quantus™ QRC (see section 2.3).

The two netlists can be simulated by SPICE simulators. The simulator connects high and low voltage nets by the substrate network if the net names in the substrate netlist equals the relevant nets in the extracted netlist. Consequently, these simulations can predict the influences of the high voltage switching on the low voltage node prior to fabrication.

4.3 Measurements of Coupling onto the Handle Wafer

To investigate the accuracy of the automated substrate network as described in section 4.2, the substrate network parameters were measured and compared to the calculated values and the values simulated with TCAD as described in subsection 4.1.1 and subsection 4.1.2, respectively.

4.3.1 Impedance Measurements of substrate network parameters

Impedance measurements were performed by a ModuLab®XM ECS system to determine the output impedance of the implemented three-state high voltage pulse generator. So called *Constant Level Impedance* measurements were performed in sample and reference mode which calibrates the measured value with an internal reference. An alternating voltage is applied with frequencies from 10 Hz to 1 MHz. The amplitude is set with respect to the load and is noted in the sections below. The software of the measurement equipment can calculate the impedance and the phase from the measured voltage and current values and returns the bode plot for the measurement. An AC hum at 50 Hz and errors at high frequencies due to the measurement equipment are known errors with this setup [123].

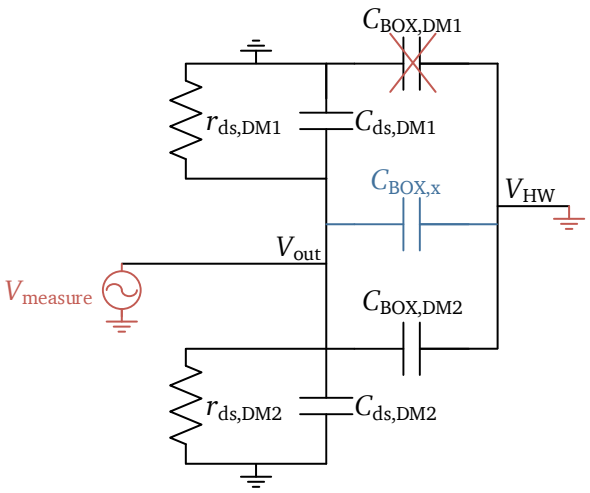


Figure 4.10.: Simplified small signal equivalent circuit of the measurement of the impedance between the handle wafer and the output of the inverter. Connection of measurement equipment is shown in red. The impedance $Z_{\mathrm{out,gnd}}$ is measured.

To measure the output impedance of the inverter and to draw conclusions about capacitances of the output node to the handle wafer is not straightforward since parasitic capacitances and resistances of the inverter can influence the measurement. The small signal equivalent circuit of the inverter including its capacitive coupling to the handle wafer is shown in Appendix D. To be able to draw conclusions on the capacitive coupling of the output transistor DM2, the applied voltage has to be much lower than the threshold voltage of the DMOS devices. By doing so, the DMOS transistors are switched off and their transconductances can be neglected. Therefore, the small signal equivalent circuit simplifies to the circuit shown in Figure 4.10. It includes an extra capacitance $C_{\mathrm{BOX,x}}$, which is the sum of other active tubs within the device wafer of the HVIC whose n^+-substrate is connected to the output node V_{out} such as pad structures for example.

The two connections of the ModuLab®XM ECS measurement system are connected to the output node of the inverter and to the handle wafer, respectively. The input clock signals of the inverter $\mathrm{clk}_{+\mathrm{HV}}$, $\mathrm{clk}_{-\mathrm{HV}}$ and $\mathrm{clk}_{\mathrm{GND}}$ are maintained at zero volts and therefore, the output transistors are switched off. The high

voltage supply pads are connected to ground. The amplitude of the measurement is set to 0.1 V_{rms} which is far below the threshold voltage of the high voltage DMOS transistors, which is larger than1.5 V. By connecting the handle wafer to ground, the capacitance $C_{BOX,DM1}$ between the drain of the high-side DMOS transistor DM1 and the handle wafer is shortened.

For the explained measurement setup, the impedance between the grounded handle wafer to the output node of the inverter $C_{out,gnd}$ is shown in Figure 4.11. For this frequency range, it can be fitted with an error of 0.05 to 17.36 pF.

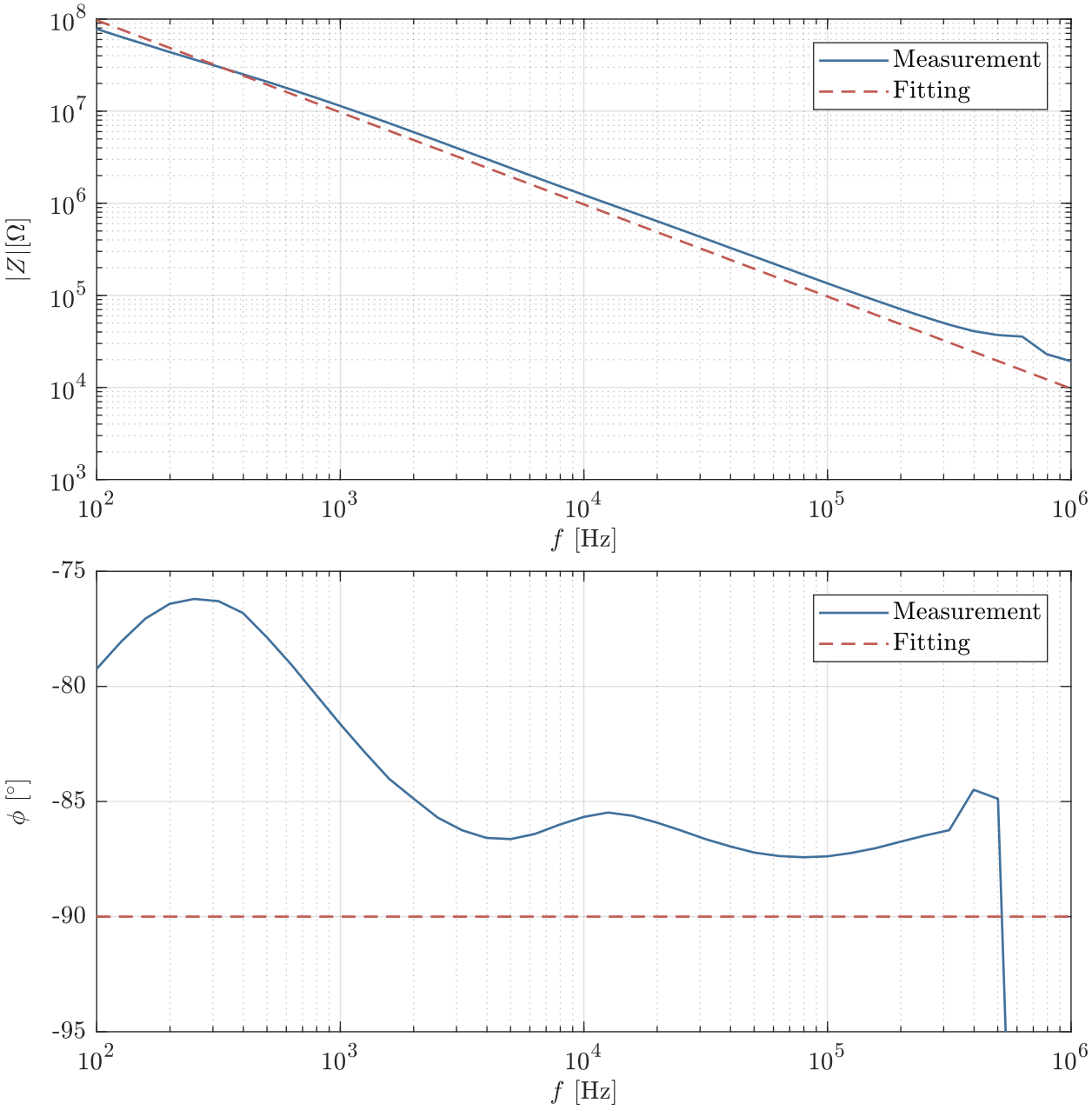


Figure 4.11.: Bode plot of the impedance of the the handle wafer to the output node of the inverter. Measurement was performed with 0.1 V_{rms}. The impedance was fitted with the data-modulus method to 17.36 pF.

Due to the measurement setup, the measured impedance includes parasitic capacitances and output resistances of the DMOS transistor as shown in Figure 4.10. The capacitance and resistance of the output transistors were obtained from simulations to be equal to $C_{\mathrm{ds,DM1,2}} = 1.67\,\mathrm{pF}$ and $r_{\mathrm{ds,DM1,2}} = 60.81\,\mathrm{G\Omega}$, respectively. The output resistance $r_{\mathrm{ds,DM1,2}}$ of the DMOS transistors can be neglected within the parallel connection of $r_{\mathrm{ds,DM1,2}}$ and $C_{\mathrm{ds,DM1,2}}$ for subthreshold operation. Hence, the measured capacitance $C_{\mathrm{out,gnd}}$ is given by

$$C_{\mathrm{out,gnd}} = C_{\mathrm{BOX,DM2}} + C_{\mathrm{BOX,x}} + 2C_{\mathrm{ds,DM1,2}}. \tag{4.17}$$

The coupling capacitance $C_{\mathrm{out,HW}}$ between the output node V_{out} and the handle wafer V_{HW} is the capacitance across the buried oxide of all n^+-regions on the HVIC that are connected to the output node

$$C_{\mathrm{out,HW}} = C_{\mathrm{BOX,DM2}} + C_{\mathrm{BOX,x}}. \tag{4.18}$$

It can be calculated to 14.02 pF and is dominated by $C_{\mathrm{BOX,DM2}}$ due to the large size of the high voltage output transistor DM2.

For the measurement setup shown in Figure 4.10, the large capacitance of the high-side output transistor DM1 is shortened and hence not measured. This can be validated by changing the measurement setup so that the voltage is applied to the handle wafer as shown in Figure 4.12. The impedance $Z_{\mathrm{HW,gnd}}$ can be fitted with a capacitance $C_{\mathrm{HW,gnd}}$ to 27.25 pF as shown in Appendix E.

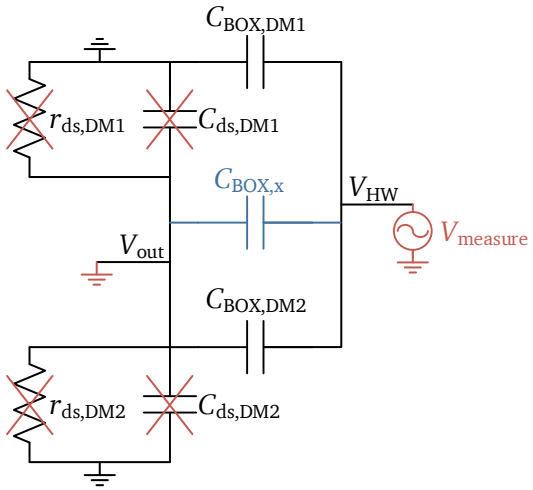


Figure 4.12.: Simplified small signal equivalent circuit of the measurement of the impedance between the handle wafer and the output of the inverter. Connection of measurement equipment is shown in red. The impedance $Z_{\mathrm{HW,gnd}}$ is measured.

As shown in Figure 4.12, the measured capacitance $C_{\mathrm{HW,gnd}}$ can be regarded as the parallel connection of $C_{\mathrm{BOX,DM1}}$, $C_{\mathrm{BOX,DM2}}$ and $C_{\mathrm{BOX,x}}$ and can be simplified to

$$C_{\mathrm{HW,gnd}} = C_{\mathrm{BOX,DM1}} + C_{\mathrm{BOX,DM2}} + C_{\mathrm{BOX,x}} = 2C_{\mathrm{BOX,DM}} + C_{\mathrm{BOX,x}} \tag{4.19}$$

since the capacitances of the two DMOS transistors DM1 and DM2 to the handle wafer are equal due to the same layout size of the transistors. Inserting Equation 4.18 in Equation 4.19 results in

$$C_{\mathrm{BOX,DM}} = C_{\mathrm{HW,gnd}} - C_{\mathrm{out,HW}} \tag{4.20}$$

This leads to a value of 13.23 pF for the capacitance of the high voltage output transistor to the handle wafer. Due to the dominance of the area of the high voltage output transistor, this value lies 5.36 %

below the value of 13.98 pF simulated with TCAD. Thus, the correctness of the measurement can be confirmed.

The constant level impedance measurements were also performed for the impedance between the handle wafer and the low voltage supply for analog circuitry V_{DDa} and digital circuitry V_{DDd}, respectively. Again, the amplitude of the measurement was set to 0.1 $\mathrm{V_{rms}}$ to not activate connected transistors during the measurement.

A comparison of the values calculated with Equation 4.9 and Equation 4.10, their correction as described in subsection 4.1.2, values extracted from TCAD simulations as well as measurement values can be found in Table 4.1. The values were calculated for the parallel connection of all $C_{\mathrm{BOX,i}}$ and R_{i3} for all extracted areas, respectively.

It can be seen that the measured capacitance between the inverter output and the handle wafer $C_{\mathrm{out,HW}}$ is 5.21 % smaller than the TCAD simulated value. This error can be due to inaccurate simulation models which were used to determine the parasitic capacitances within the measurement.

Table 4.1.: Comparison of substrate parameters for analytic equations, corrected values for analytic equations, TCAD simulation and measurement.

	Analytic equations	Corrected analytic equations	TCAD	Measurement
$C_{\mathrm{out,HW}}$ [pF]	13.64	14.66	14.79	14.02
$R_{\mathrm{out,HW}}$ [Ω]	29.02	8.73	10.49	-
$C_{\mathrm{VDDa,HW}}$ [pF]	5.09	5.88	6.63	7.51
$R_{\mathrm{VDDa,HW}}$ [Ω]	77.68	6.56	19.58	-
$C_{\mathrm{VDDd,HW}}$ [pF]	10.01	15.22	13.87	14.19
$R_{\mathrm{VDDd,HW}}$ [Ω]	38.02	2.44	10.75	-

However, as Table 4.1 shows, the presented analytic equations can be used to determine the parameters that influence the substrate coupling most. The approximation can be improved by taking the fringing capacitances, which were determined by TCAD simulations, into account. Hence, the substrate network parameters can be used to simulate the influences of the high voltage switching on low voltage circuitry.

4.3.2 Voltage Measurements on Handle Wafer

To measure influences on the handle wafer, the bottom contact of the die has to be floating. However, by contacting the handle wafer for measurements with a wafer probe and a connecting oscilloscope, the floating handle wafer contact is loaded. As a consequence, the measurable voltage at the handle wafer V_{HW} is damped due to the connected load. Measurements were performed with an oscilloscope of type Textronik TDS2024C. The high output voltage V_{out} was probed by a high voltage probe of type "TT-HV 250" from TESTEC Elektronik GmbH with an attenuation ratio of 100:1 [104]. The voltage at the handle wafer V_{HW} was probed with a needle at the wafer prober.

Figure 4.13 shows the output of the high voltage inverter V_{out} and the corresponding handle wafer voltage V_{HW} for an output load of 1 nF and ±200 V for the high voltage supply. The maximum inverter frequency of 5 kHz is applied for these measurements. It can be seen that V_{HW} is directly related to the switching inverter output.

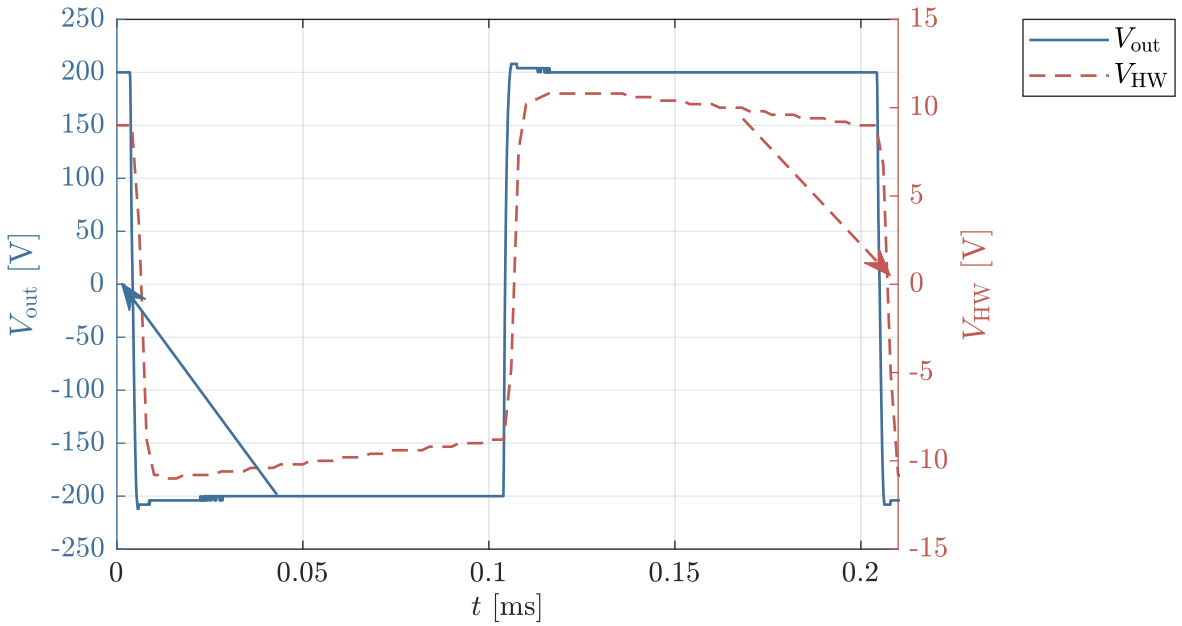


Figure 4.13.: Measurements of output voltage V_{out} and the damped handle wafer voltage V_{HW} for ±200 V, an output load of 1 nF and an output frequency of 5 kHz.

As shown in Figure 4.14, the damped voltage at the handle wafer scales with the maximum output voltage of the inverter. The damping factor

$$D = \frac{V_{\text{HW,p}}}{V_{\text{out,p}}} \tag{4.21}$$

is slightly dependent on the output voltage and varies between 4.89 % for ±50 V to 5.29 % for ±200 V.

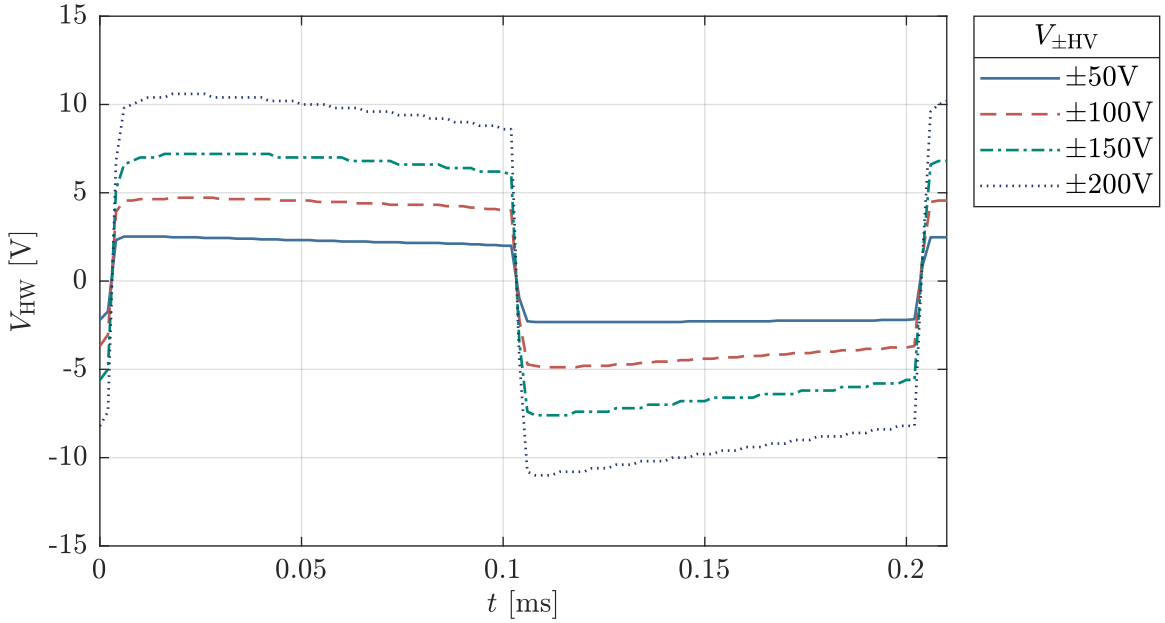


Figure 4.14.: Measurements of the damped handle wafer voltage V_{HW} for different high supply voltages.

To compare the measured waveform with simulations, the load due to the measurement setup has to be determined. It has to be taken into account while generating the netlist for SPICE simulations. The load comprises five parallel components as shown in Figure 4.15: the capacitances of the packaged IC

on the PCB C_{PCB}, the probe C_{probe}, the BNC cable C_{BNC} which connects the probe to the oscilloscope as well as the input impedance of the oscilloscope. The latter consists of the parallel connection of C_{scope} and R_{scope}. Constant level impedance measurements of the different components were performed by a ModuLab®XM ECS system. The results are shown in Appendix F. Table 4.2 lists the fitted parameters. A total load of $C_{\mathrm{load}} = 250.05\,\mathrm{pF}$ in parallel to $R_{\mathrm{load}} = 1.21\,\mathrm{M\Omega}$ was measured.

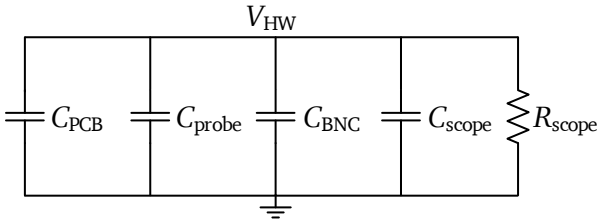


Figure 4.15.: Equivalent circuit of the experimental setup. The components represent the load connected to the handle wafer during measurement.

Table 4.2.: Fitted impedances from impedance measurements of the measurement equipment setup.

Parameter	Value	Reference
C_{PCB}	98.88 pF	Figure F.1
C_{probe}	30.82 pF	Figure F.2
C_{BNC}	98.82 pF	Figure F.3
C_{scope}	21.53 pF	Figure F.4
R_{scope}	1.21 MΩ	Figure F.4

The substrate network for the implemented HVIC, described in section 4.1, was extracted from the layout by the method presented in section 4.2. In parallel, the post-layout of the IC was extracted using the tools of the conventional design flow. These two netlists were combined and simulated. To validate the measurements of the voltage on the handle wafer, the handle wafer was charged with the described load of the measurement setup.

Figure 4.16 shows the comparison of the damped handle wafer voltage V_{HW} for an output peak voltage of ±200 V at an output frequency of 5 kHz. It can be seen that the measurement can be well predicted by the SPICE simulation. The maximum voltage in the SPICE simulation exceeds the measurement by 0.42 V which equals 3.68 %. The slope of the simulated voltage is slightly higher than the measured value. This can be due to the bandwidth of the utilized oscilloscope or variations within the substrate network. Small variation within the load also influences the conformity between simulation and measurement.

4.4 Influences of High Voltage Pulses on Spread Spectrum Clock Generator

After showing that the high voltage inverter couples to the handle wafer, its influences on low voltage circuitry are analyzed in the following. In thick SOI dies, all tubs have a highly doped n^+-region on top of the BOX. The high doping is conducted next to the trenches to the wafer surface, as shown in Figure 4.5. Thus, the bulk of each individual tub can be contacted individually. For low voltage tubs, the substrate within the tubs is mostly connected to the low voltage power supply to reverse bias parasitic diodes to the n-doping. Any change on the handle wafer can therefore couple onto the low voltage power supply V_{DD}.

Measuring the influences of the high voltage switching on the low voltage power supply is difficult. On the one hand, this is due to the fact that the measurement equipment loads the supply voltage. Due to the capacitive behavior of the measurement setup, as shown in subsection 4.3.2, the low voltage supply is

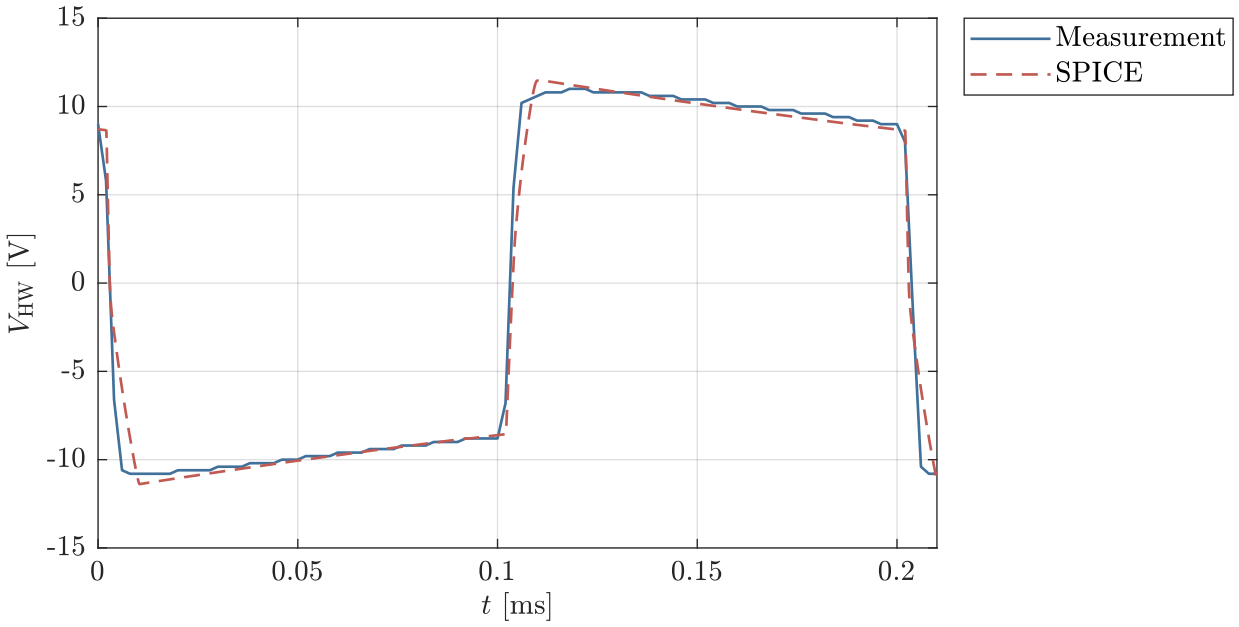


Figure 4.16.: Comparison of measurement and SPICE simulation for the damped handle wafer voltage V_{HW} for an output peak voltage of ±200 V, an output frequency of 5 kHz and an inverter load of 1 nF.

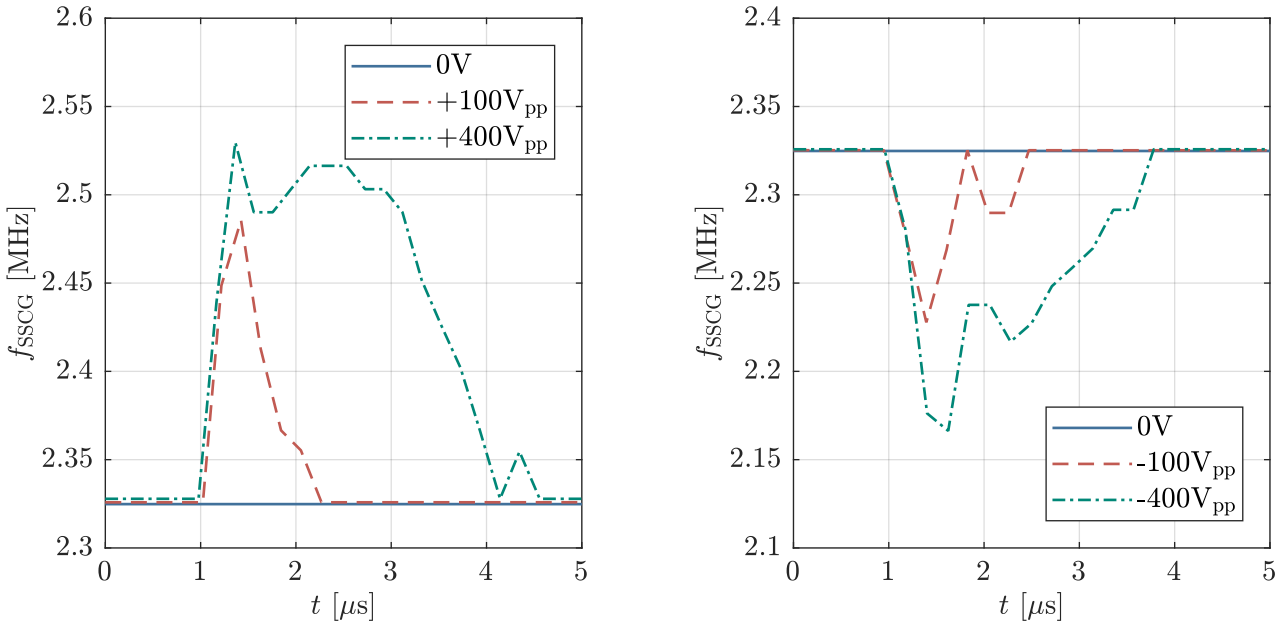
stabilized during the measurement. As a result, the measurable influences reduces. On the other hand, the coupling takes place on the bottom of the active wafer where it cannot be contacted. Resistive drops across wires and vias up to the point where the measurement tip can probe the signal additionally falsify the measurement result.

The interferences of the high voltage coupling can be measured at the outputs of low voltage circuitry. Digital outputs are particularly suitable as they are not distorted by the additional load of the measuring tip as long as the output buffer can drive the load. Figure 4.17 shows the measured influences of the high voltage switching on the implemented spread spectrum clock generator for different high supply voltages. It can be seen that the frequency of the SSCG changes with rising and falling edges of the inverter output. The frequency changes at a peak of +7.37 % for a maximum output voltage of +50 V and increases to +9.05 % for a maximum output voltage of +200 V. The change is smaller for falling edges. It is -3.88 % or -6.47 % for falling edges with an output voltage of -50 V and -200 V, respectively.

4.4.1 Coupling of Interference Signals at the Handle Wafer

To determine that the influences of the f_{SSCG} are caused by variations of the substrate handle wafer voltage, an AC voltage was applied to the handle wafer. In this case, the inverter output voltage of one die was connected to the handle wafer of a second die to obtain the slew rate of the signal. For this measurement, the supply voltages for the high inverter were chosen to ±50 V. The output of the inverter was loaded with a capacitance of 1 nF with highest possible slew rates.

Figure 4.18 shows the measured output frequency of the SSCG with an alternating substrate handle wafer voltage. First of all, it can be seen that the extracted frequency f_{SSCG} changes for rising as well as for falling edges of the handle wafer voltage. From this, it can be concluded that high voltage pulses from an inverter can interfere low voltage building blocks via the handle wafer substrate. Just as with



(a) Rising edge.

(b) Falling edge.

Figure 4.17.: Influences of coupling of the switching inverter output on the clock frequency f_{SSCG} of the spread spectrum clock generator with PRN = 1 for different high supply voltages for an output load of 1 nF.

the measurement of the frequency change of the SSCG by high voltage switching on the same die in Figure 4.17, the influence of the rising edge is higher than for falling edges for the direct coupling on the handle wafer. This can be due to the higher slew rates for the positive edge compared to the negative as denoted in subsection 3.4.1. The different degrees of coupling can also be caused by the fact that some transistors leave their operating point as a result of the V_{DD}-changes and thus the gain of the circuit changes drastically.

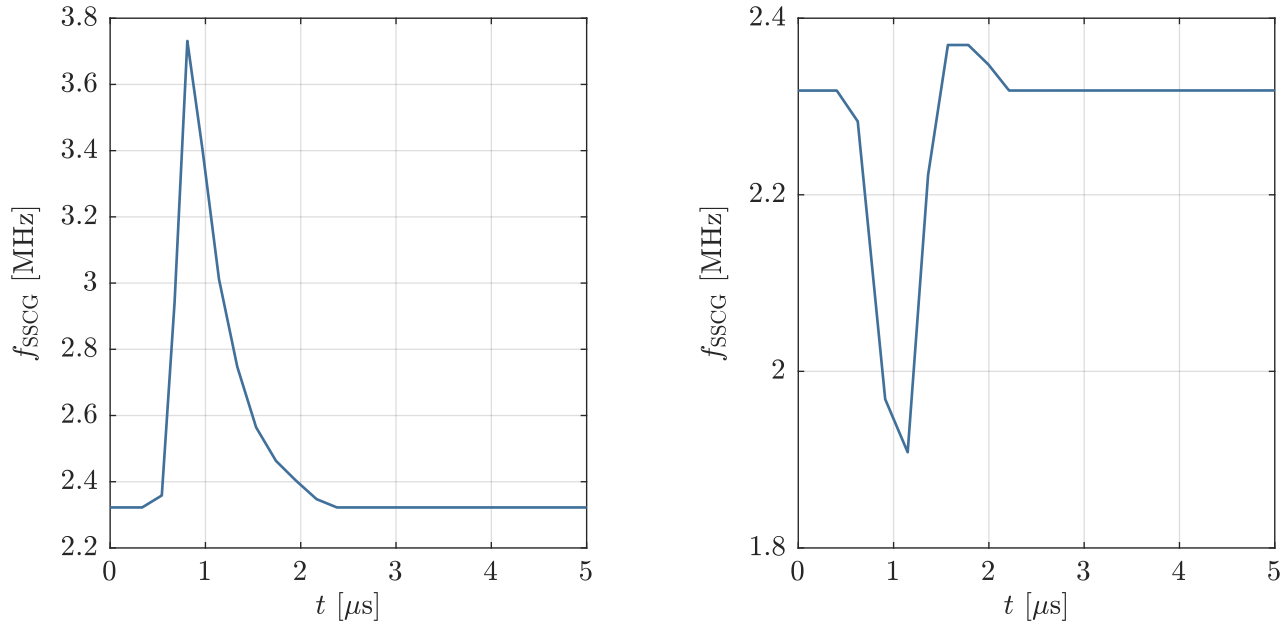
Compared to the measured influences of the high voltage inverter within the same die, as shown in Figure 4.17, the frequency change of the spread spectrum clock generator caused by direct control of the handle wafer voltage is higher, both for rising as well as falling edges. Table 4.3 lists the minimum and maximum measured frequency for the rising and falling edges for high supply voltages of ±50 V. The relative error from the nominal frequency value of $f_{SSCG,nom} = 2.31\,\text{MHz}$ can be calculated by

$$\epsilon = \frac{f_{SSCG,peak} - f_{SSCG,nom}}{f_{SSCG,nom}}. \tag{4.22}$$

From this it can be concluded that the coupling on the handle wafer of the inverter output is damped by the substrate network as well as the packaging.

4.4.2 Prediction of Influences by Simulation

With the help of the presented substrate network and its automated extraction as described in section 4.1 and section 4.2, the coupling of the high voltage pulses from the fully integrated three-state inverter on the same die can be predicted by SPICE simulations. For the implemented SSCG, special focus has to be put on PMOS transistor M11 of stage four within the voltage-to-current converter which was introduced in



(a) Rising edge.

(b) Falling edge.

Figure 4.18.: Influences of the clock frequency f_{SSCG} of the spread spectrum clock generator with PRN = 1 by AC pulses between -50 V and +50 V of the handle wafer voltage.

Table 4.3.: Comparison of output frequency chances caused by inverter coupling and handle wafer voltage changes for changes of -50 V and +50 V. The nominal frequency without any coupling is 2.31 MHz.

	HW coupling		Inverter coupling	
	$f_{SSCG,peak}$ [MHz]	ϵ [%]	$f_{SSCG,peak}$ [MHz]	ϵ [%]
Rising edge	3.73	+60.78	2.49	+7.37
Falling edge	1.91	-17.67	2.23	-3.88

Figure 3.32 in subsubsection 3.3.2.4. Its bulk and therefore the substrate of its active tub is not connected to V_{DD} but to its source. Consequently, the parasitic charge of the high voltage pulse generator directly couples onto this node. Due to the structure of the voltage-to-current converter, this coupling has a significant impact.

If possible, the substrate network should be simulated in combination with the parasitic extraction of the complete SoC. However, for high voltage ICs, the simulation tools often fail to converge due to the high slew rates of high voltage pulse generators. In this case, output voltage waveform of the inverter can be saved and used as an input voltage source for the post-layout simulation of the low voltage components. In this case, the resistance to the V_{DD}-pad has to be extracted from the layout of the complete SoC.

The exact knowledge of the connection of the supply voltage is necessary for the simulation, since parasitic charge across the substrate network couples into the supply voltage V_{DD}. The output resistance of the source as well as the resistances of the connecting wires play a decisive role in the accuracy of the prediction of the coupling by the simulation. For the implemented SoC, a worst case approximation can be obtained by analyzing the V_{DD} tracks on the HVIC. The longest path for the supply voltage of the analog

building block V_{DDa} adds a total resistance of 7.37 Ω. The most critical path for the digital components of V_{DDd} adds a resistance of 29.64 Ω. In this calculation, the contact resistances were neglected. Furthermore, the resistance of the n^+-regions from the top of the active tub to the bottom of the device wafer where the handle wafer is couples to, are negligible.

By introducing these values into the V_{DD}-path and adding series inductances of 3 nH for the bond wires in the schematic, the interferences of the high voltage pulses on the spread spectrum clock generator can be simulated. Figure 4.19 and Figure 4.20 show the comparison of simulation results and measurements for a rising and a falling edge of 400 V_{PP}, respectively. First, it can be observed that the simulated nominal frequency of the spread spectrum clock generator f_{SSCG} is higher for than the measured device. For a better comparability, two y-axes are introduced which only differ by their lower and upper limits but have the same axes scaling.

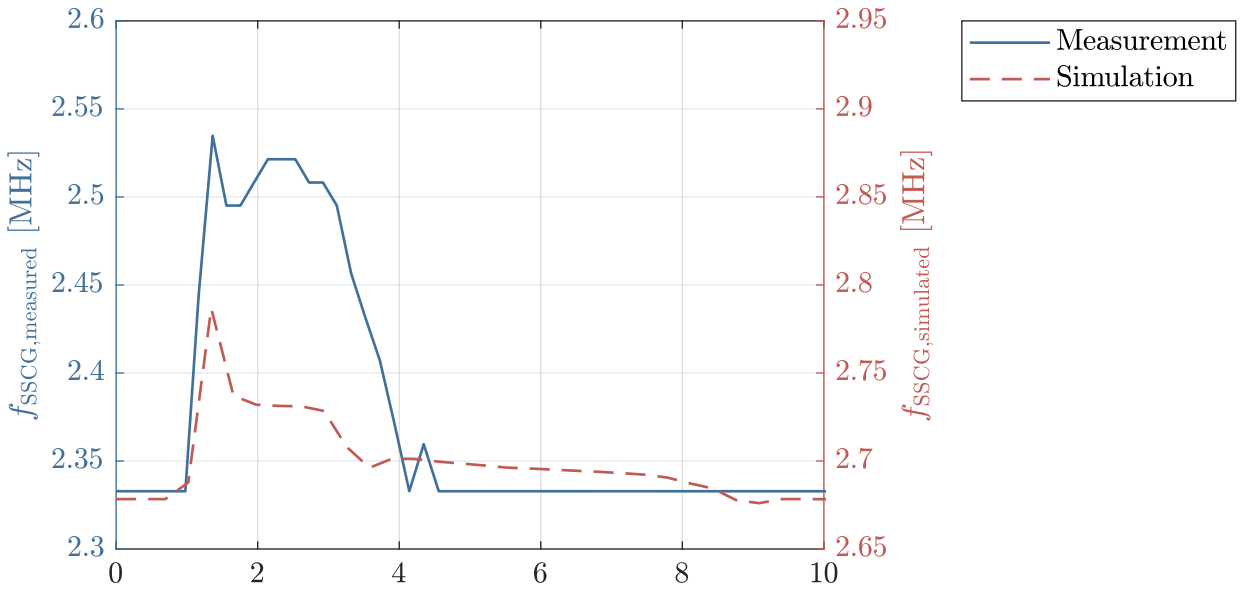


Figure 4.19.: Measurement and simulation of the spread spectrum clock frequency f_{SSCG} including substrate network for a rising edge of a high voltage pulse with a peak-to-peak voltage of +400 V_{pp} at 5 kHz. The output of the inverter was loaded with 1 nF.

As discussed in section 4.4, the measured output frequency of the spread spectrum clock generator increases for a rising edge of the inverter output. Likewise, the simulation including the extracted substrate network shows a positive deviation of the SSCG frequency, as shown in Figure 4.19. However, the error caused by the high voltage pulse both of the peak and of the total deviation over time is smaller in simulation than for the measurement. The same observations can also be made for falling edges of the inverter output voltage. As Figure 4.20 shows, the frequency deviation is negative, but in terms of magnitude and total deviation over time, it is also smaller than the measured values.

The deviations between simulation and measurement can have different causes. The previously discussed modeling of the supply voltage is just as important as the consideration of mismatch within the circuit. Unless all relevant capacitive and inductive components are taken into account in the post-layout simulation, this can also create a discrepancy between simulation and measurement. In order to obtain more accurate predictions about the influence of mixed-signal devices, further investigations with 3D field simulations are necessary. Despite these deviations, the substrate model presented in this thesis can be used to predict interferences of mixed-signal building block by ultra high voltage pulse generators on the system-on-chip.

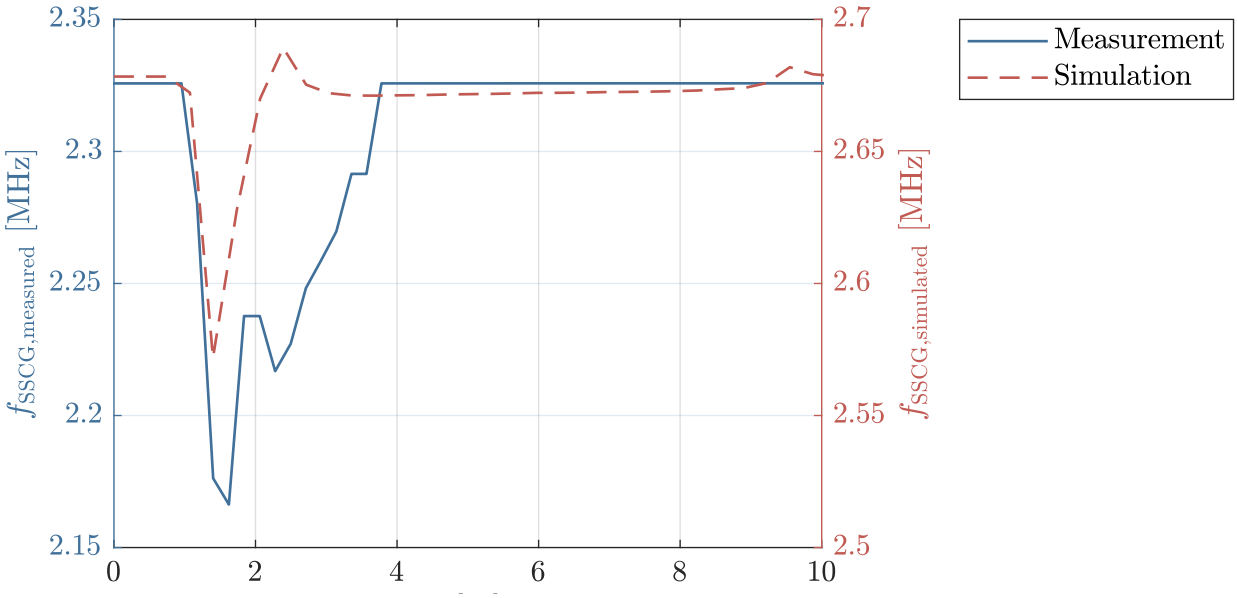


Figure 4.20.: Measurement and simulation of the spread spectrum clock frequency f_{SSCG} including substrate network for a falling edge of a high voltage pulse with a peak-to-peak voltage of -400 V_{pp} at 5 kHz. The output of the inverter was loaded with 1 nF.

4.5 Thermal Influences within the High Voltage Integrated Circuit

Apart from electrical coupling, heat dissipated by high voltage inverters can also have an influence on the operation of low voltage circuitry. Depending on the thermal resistance of the packaged IC, the temperature of the IC can vary. Compared to bulk CMOS processes, the active wafer in the SOI process has a much lower thickness of only approximately 50 µm. Since the thermal conductivity of electrically conductive materials is in general much higher than for isolating materials, the buried oxide inhibits the heat transfer into the handle wafer. Thus, higher operating temperatures within the device wafer of SOI ICs with switching outputs can be expected compared to bulk CMOS ICs. The influences of the higher operating temperatures on the high as well as on the low voltage components can be simulated.

The influences of the three-state high voltage inverter on the spread spectrum generator for the HVIC presented in section 3.4 are discussed in this section. The temperature of the IC can be measured by a pn-junction within ESD protection diodes of digital input pads. Figure 4.21 shows the schematic of measurement across the ESD protection diodes. The attached high ohmic input resistance of the input buffer within the digital pad is neglected. For the measurement, a current source with 1 mA is connected to the input pad. The voltage at the input pad across the diode $-V_D$ is dependent on temperature due to the temperature dependence of the pn-junction of the diode.

To evaluate the temperature of the IC in operation mode, the diode voltage is measured for reference purposes at different ambient temperatures T within a heat oven. Figure 4.22 shows the measurement for calibrating the temperature measurement. It can be linearly fitted with an R^2 accuracy of 0.999 by

$$V_{Diode}(T) = -2.16\,\frac{\text{mV}}{\text{°C}} \cdot T + 711.74\,\text{mV}. \tag{4.23}$$

The standard deviations of the y-axis intercept and the slope are ± 1.85 mV and ± 0.02 mV/°C, respectively.

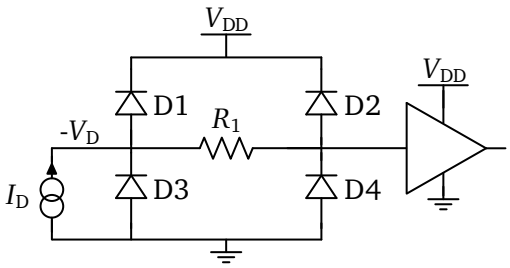


Figure 4.21.: Schematic of the ESD protection of a digital input cell. The temperature dependency of the pn-junction within the diodes can be used to measure the temperature on the IC.

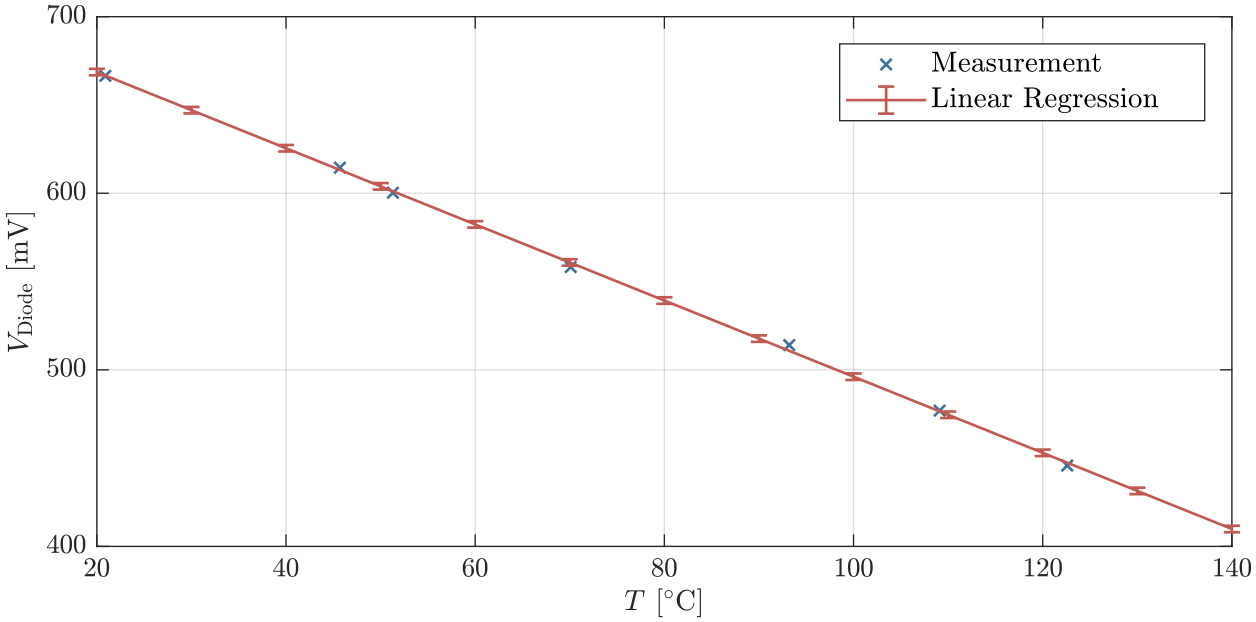


Figure 4.22.: Temperature reference for calibration of temperature measurement.

For the temperature measurements with the fabricated HVICs, the intended time multiplexing, as explained in section 3.1, was applied to the inverter. Hence, the high voltage output was switched on for 2 ms at 5 kHz and switched off for 8 ms. The voltage V_D was measured in steady state for different ouput loads and high supply voltages. The temperature on the IC was calculated by Equation 4.23. The results are shown in Figure 4.23. As expected, the IC temperature increases with the peak voltage of the inverter. Furthermore, the temperature is increasing with the output capacitance due to higher output currents and hence higher power consumption within the HVIC. With the given time multiplexing and an output capacitance of 10 nF, the temperature of the IC increased up to 81.64 °C in steady state.

For the presented HVIC, the output frequency of the spread spectrum clock generator f_{SSCG} changes due to the power dissipation of the inverter. Figure 4.24 shows that the lower frequency f_0 of the SSCG changes from 2.51 MHz at 0 V to 4.31 MHz at ±200 V inverter output voltage, respectively. The extracted operating temperature of the SSCG rises by 23.38 K for the applied voltage range.

The prediction of the temperature change due to the power loss of, inter alia, high voltage circuits or power transistors prior to fabrication has already been extensively researched and will therefore not be further investigated in this work. Various approaches for determining the operating temperature of an IC have been presented. There are some standalone programs for electro-thermal co-simulations such as,

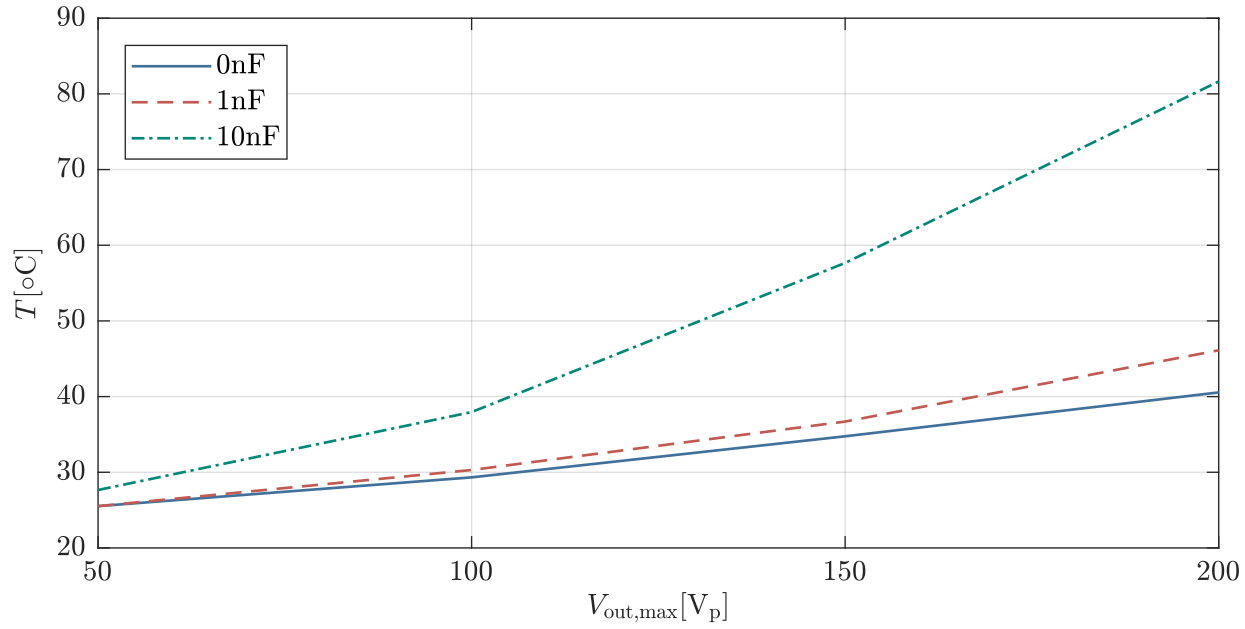


Figure 4.23.: Measured chip temperature for different output loads. The output was switched with a frequency of 5 kHz and a duty cycle of 0.2 .

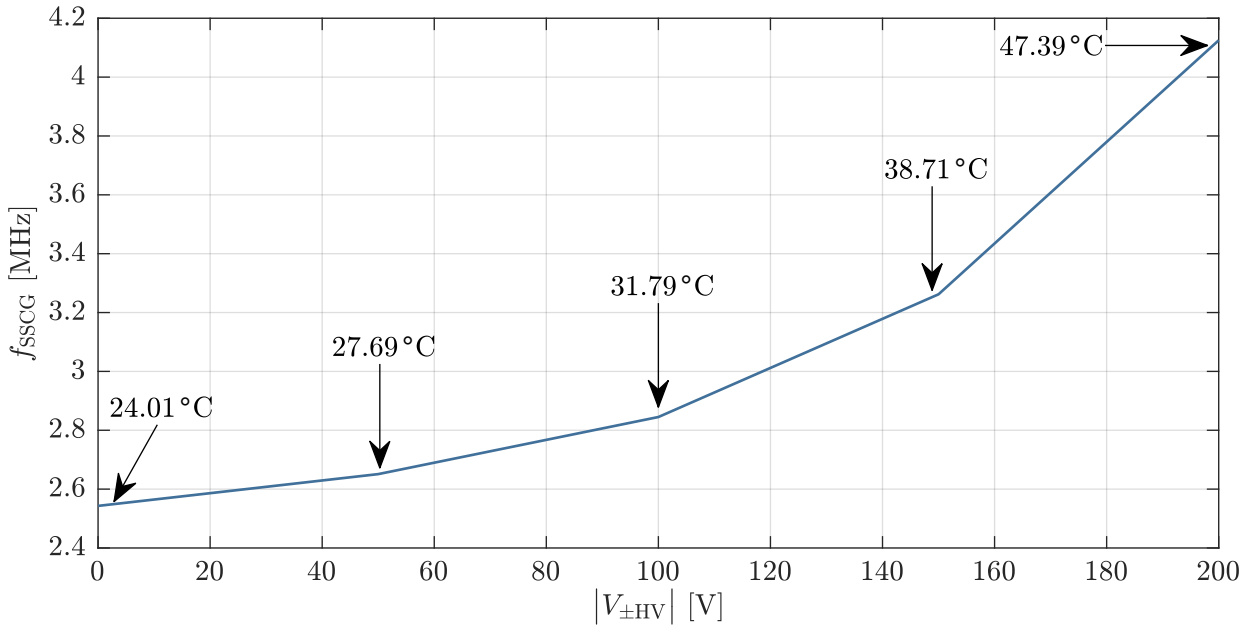


Figure 4.24.: Measured output frequency of the SSCG f_{SSCG} for a PRN of 0 with respect to the high supply voltage of the inverter. The measurement was performed with the presented time multiplexing scheme and an inverter output load of 1 nF.

for example, ANSYS® [124] and Magwel® [125]. The IC Design software provider Cadence® offers a separate tool, called *Legato™ Reliability Solution* to investigate electro-thermal issues. Other efforts are being made to integrate temperature of the chip into the conventional IC design process [126, 127].

4.6 Summary

In this chapter, the influences of alternating high voltages on circuits with low supply voltages were investigated. Apart from electrical coupling, power dissipation within the high voltage inverter can have a significant impact on low voltage circuitry. Due to the SOI substrate, heat cannot be easily dissipated to the handle wafer. Therefore, high temperatures can be expected during the operation of the inverter. Low voltage components are therefore operated in temperature ranges that are not usual for them. This has to be taken into account during the design phase of the IC.

In addition to capacitive and resistive parasitics on the chip, which are covered by the parasitic extraction implemented in the conventional design flow, electrical coupling via the substrate has proven to be a crucial source of influence. For thick SOI processes, the substrate handle wafer represents a common node onto which charge can capacitively couple from switching high voltage nodes. From there, charge can couple to the device wafer into any low voltage active tub.

As previous research showed, a relevant part of the coupling current in SOI flows in the active wafer substrate close to the buried oxide [20]. Therefore, it is suggested to introduce a highly doped layer on top of the buried oxide which is connected to an appropriate DC voltage such as ground or V_{DD} for p-substrate and n-substrate, respectively. Charge is captured by this highly doped layer and hence, the substrate is capacitively shielded. By implication, a highly doped region above the BOX can introduce high parasitic currents into the handle wafer if it is connected to a high voltage switching output.

Quasi-vertical DMOS transistors in n-doped SOI processes have their drain connected at the highly doped n^+-region above the buried oxide. These DMOS transistors introduce high coupling to the handle wafer when they are used as low-side output transistors in high voltage inverters. An equivalent model of the substrate is presented. Analytic equations for the parameter values as well as correction factors obtained by TCAD simulations are presented. The substrate network can be generated automatically by a SKILL® based program.

Constant level impedance measurements for the impedance between the output of the implemented inverter and the handle wafer revealed a good conformity with the values for the analytic equations as well as TCAD simulation. The coupling to the handle wafer could be reproduced well in SPICE simulations with the help of the extracted substrate netlist.

Likewise, it was shown that changes of the handle wafer voltage can interfere the functionality of low voltage circuitry. The voltage change on the handle wafer is usually capacitively coupled to the supply voltage V_{DD} of low voltage circuitry. Although measuring the influences on the low voltage power supply caused by the high voltage switching is not feasible, the influences can be made visible by the change of digital outputs as they are not distorted by the additional load of the measuring tip. Measurements revealed an increase of the frequency of the implemented spread spectrum clock generator by up to 9.05 %. These changes can be predicted with the extracted substrate netlist. Therefore, an exact knowledge of the connection of the supply voltage is necessary for the simulation. Output resistance of the source as well as resistances of the connecting wires have to be taken into account.

It has been shown that the equivalent circuit model presented in this chapter can be used to estimate the effects of switching high voltages on low voltage circuitry. This approximation can be implemented in the design phase of the chip. It allows errors and system degradation to be detected at an early stage of the design phase. Consequently, the model can also be used to make circuits more robust against high voltage transients.

5 Interference-Aware Design of SoCs with Ultra High Voltage Pulse Generators

The investigations of the fabricated SoCs in chapter 4 showed that the influences of a high voltage pulse can have a significant impact on the behavior of low voltage functionalities. The interferences can be attributed to electronic coupling by the high voltage pulses as well as to heat transfer of the power dissipated from the inverter.

In the design of SoCs, preventative measures can be taken at various points during the implementation to increase the robustness and reliability of the HVICs and to minimize the effects of high voltage pulses on low voltage nodes. As already described in chapter 2, the selection of the technology and thus of the physical isolation technique has a considerable influence on possible couplings. Non-technical factors such as cost and availability often play a crucial role in the decision. Once the technology is chosen, IC designers can further minimize coupling effects within the SoC. Figure 5.1 shows the different implementation steps during which considerations can help reduce the influences of high voltage components on low voltage circuitry. During the IC design, architectural decisions concerning the transistor level implementation as well as layout considerations can minimize the influences between two different voltage level domains. By taking into account a few points during the planning of the packaging, the impact between two voltage level domains can be minimized or even eliminated so that the components can be manufactured on an IC without influencing each other.

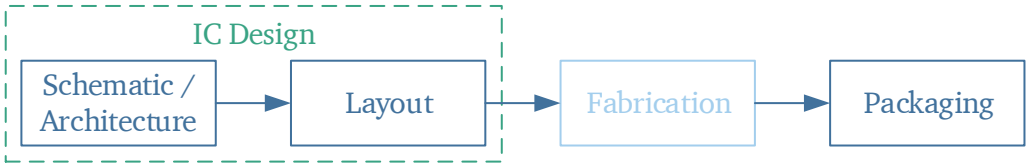


Figure 5.1.: Block diagram of the different implementation steps during which considerations can help to reduce the influences of high voltage components on low voltage circuitry.

5.1 Circuit Design Considerations

During the design of a system-on-chip with an on-chip high voltage pulse generator, first measures can already be taken to reduce the influences between building blocks with different voltage supplies. For ICs based on SOI wafer with thick buried oxide and n-doped substrate, high voltage substrate coupling can be avoided if the n^+-region above the BOX is connected to a DC voltage. For high voltage inverters, it would be aspired to do without any n-channel DMOS transistor whose drain is connected to a switching output. If unavoidable, the following topics can be considered to minimize interferences on low voltage circuitry.

5.1.1 Robustness against Power Supply Changes

For n-doped SOI wafer, the substrate of low voltage circuitry is mostly connected to the low voltage power supply V_{DD} to reverse bias parasitic diodes within the tub. Hence, surrounding tubs as well as the handle wafer substrate are shielded from changes within the low voltage circuitry.

Charge that is coupled to the handle wafer from, for example high voltage pulse generators, however, can be coupled via the BOX capacitance to the supply voltage of the low voltage components. To reduce the coupling, capacitances at the low voltage power supply can be implemented on chip to stabilize V_{DD}. Hence, voltage ripples on V_{DD} get reduced and the functionality of the low voltage building block is maintained.

Another way to reduce the effects of high voltage transients on low voltage circuits is to make the circuit itself more robust to voltage fluctuations. In general, electrical systems can be mainly described by their transfer function $A(s)$

$$A(s) = \frac{\partial v_{OUT}}{\partial v_{IN}}. \tag{5.1}$$

In addition, other influences, such as variations of the supply voltage, have an effect on the output as shown in Figure 5.2. Again, a transfer function $A_p(s)$ can be specified. The Power Supply Rejection Ratio (PSRR) is a measure of how much variations in the low voltage supply V_{DD} distort the desired transfer function

$$\text{PSRR} = \frac{A(s)}{A_p(s)} \quad [128]. \tag{5.2}$$

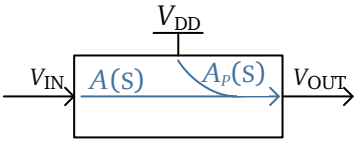


Figure 5.2.: General block diagram of an electric circuit with input and power supply transfer functions (adapted from [128]).

For an interference-aware design of SoCs with integrated high voltage pulse generators, it is important to chose architectures with high PSRR for the low voltage circuits. In literature, many low voltage building blocks have been reported with special focus on high PSRR. Among others, these include bandgap references [129], low-dropout regulators [130] as well as operational transconductance amplifiers [128].

5.1.2 Temperature Stable Circuitry

As described in section 4.5, the output transistors of output stage of the high voltage pulse generator dissipate a significant amount of power which dissipates as heat. Low voltage building blocks on the same die can suffer from high operating temperatures. Faulty results or even failures of the low voltage components can be caused by the increase of the temperature.

First and foremost, care should be taken in the IC design to ensure that the HV circuits have little power dissipation, since low currents can already cause high power dissipation for the high voltages. Sufficient dead time between the control of the high-side and low-side transistors has to be considered essentially.

Despite observing the dead time, the change in the output voltage may result in undesired turn-on of the normally-off transistor. If, for example, the output of the inverter is switched to the positive high voltage supply, the high-side transistor is turned on, the low-side transistor is ideally off. However, the change in the output voltage can be coupled to the gate through the gate-drain capacitance C_{GD}. As a result, the gate-source voltage of the low-side transistor can briefly increase and even exceed the threshold voltage, whereby the transistor is turned on undesirably. Thus, there is a low-impedance path between the

positive and the negative high supply voltage. The short circuit current increases the power consumption significantly.

To prevent this, some design measures can be taken. If possible, the slew rate of the output signal should be reduced. By reducing the voltage change $\partial V_{\text{out}}/\partial t$, the current in the gate-drain capacitance C_{GD} is reduced to the same extent and thus the increase of the gate voltage. However, this limits the maximum frequency of the high voltage output stage. The same effect can also be achieved by a low impedance between the gate and the source of the output stage. For the implemented inverter of Figure 3.19, the resistor R_9 and R_5 for falling and rising edges, respectively, would have to be chosen smaller. This in turn leads to a higher power consumption when switching on the low-side or the high-side transistor, respectively. The parasitic turning on of the output transistors can also be prevented by a capacitor in parallel to R_9 and R_5, respectively. This in turn has the disadvantage that a higher charging current is needed or the switch-on of the high voltage output transistor is extended, which also limits the maximum output frequency. For the given application, therefore, the optimum tradeoff between power consumption for switching the output transistors on, output frequency and power dissipation of the inverter has to be considered by the designer.

When implementing the low voltage components, care should be taken that the circuits are designed to be temperature-stable. Especially reference currents and bandgap voltages should not only have high PSSR but also have little change over the occurring temperature range.

If, despite the possibilities mentioned here, the temperature in the IC increases too much due to the switched output voltage, the possibilities of heat dissipation can be considered. First, this can be achieved by an external cooling of the IC and second by changing the technology. Bulk processes, as described in section 4.5, generally have better heat dissipation than SOI ICs.

5.2 Layout Considerations

After an interference-aware design of the schematic implementation, different aspects can be considered in the layout phase to further increase the robustness of the IC. Basically, the analog layout rules apply in the same way for the implementation of HVICs. Especially the layout of the low voltage components should be optimized in terms of matching and parasitic influences as discussed in [131]. If available, guard rings should be placed around individual devices to obtain the most stable substrate voltage possible.

The layout of the HV transistors is usually included in the PDK of the technology. Adjustments of parameters such as e.g. width or number of center pieces are automatically adopted in the layout. It is not advisable to change the foundry's default designs, as this can lead to faulty or non-characterized devices. The same applies to the implementation of HV resistors and HV capacitors. If these are not specified in the PDK, they can be created manually with the help of good technology knowledge. Hints can be found in [22]. High-current signals should be routed on thick metal layers. If possible, they should also be routed orthogonal to other signal lines in order to exclude inductive influences.

In order to avoid parasitic influences between high voltage pulses and low voltage devices, sufficient isolation must be inserted. Junction isolation in bulk processes and trenches in SOI can reduce substrate noise, but they also require a lot of chip area. The distance between the HV and LV components on the chip should be maximized as much as possible to reduce influences [45]. In addition, metal lines can be introduced on each layer. These can be used as magnetic and inductive shielding if they are connected a DC voltage such as for example ground.

For SOI ICs, the handle wafer should be set to a fixed potential. Depending on the process, this may already be provided by a special process step of the fabrication. In this case, handle wafer contacts have to be placed in the layout.

Even though some suggestions have been made in this chapter, layout optimization techniques to minimize the influences of high voltage switching are technology as well as design specific. Hence, it is not possible to set up generally valid rules [45, p. 173].

5.3 Packaging Considerations

By following the recommendations mentioned in section 5.1 and section 5.2, the influence of high voltage switching on low voltage components should already be greatly minimized. A release of the design data to the foundry enables the production of the HV SoC.

There are a few things to consider when planning the package so that the HVIC can work properly. If the chosen SOI technology does not allow the handle wafer to be contacted from the top side of the IC, it must be taken into account when selecting the packaging. In this case, the handle wafer should be contactable from the back side. Hence, a conductive gluing on a conductive base material of the package should be chosen. In addition, bond wires of the high voltage components should be orthogonal to low voltage bond wires, preventing inductive coupling.

The packaging has a significant impact on the thermal resistance. It therefore is very important for the thermal management of the packaged IC. This must be taken into account for the operation of the HVIC.

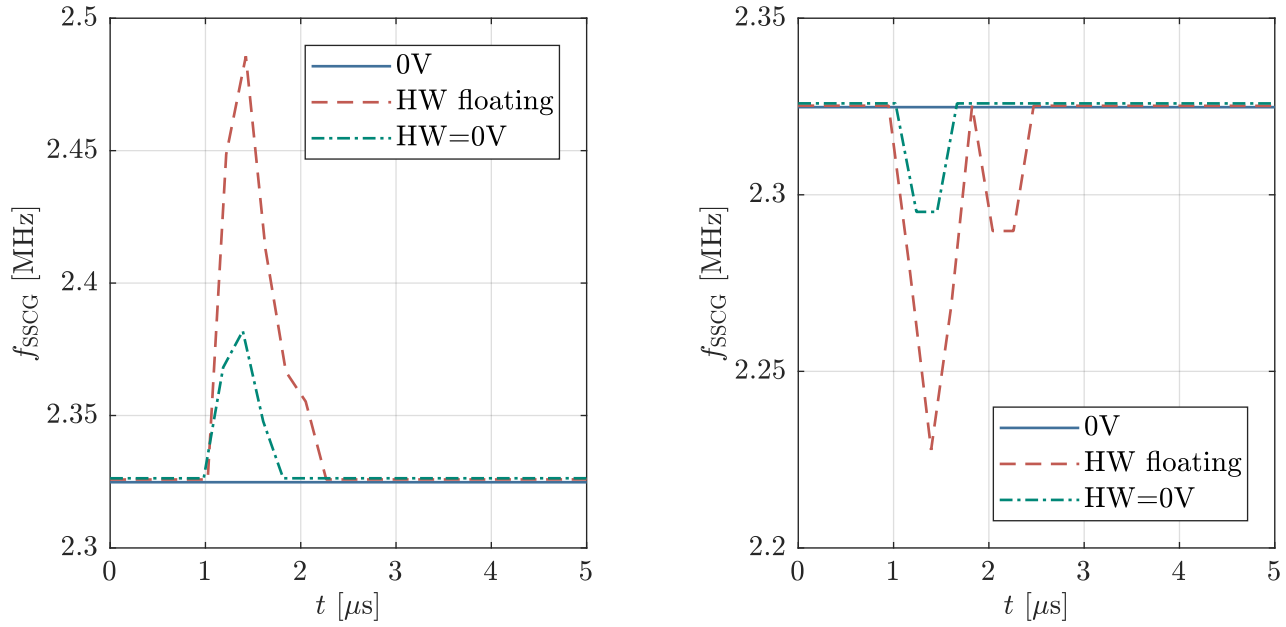
5.4 Reduced Influences on the Fabricated SoCs

After fabrication, no changes can be made in the circuit implementation nor in the layout of the IC. However, for the fabricated SoC, described in chapter 3, a significant reduction of the interferences of the ultra high voltage pulse generator could be achieved by contacting the handle wafer. Figure 5.3 shows the influences of the inverter output on the frequency of the spread spectrum clock generator for a floating handle wafer and for a grounded handle wafer. It can be seen that the influences can be reduced significantly by grounding the handle wafer. For a rising edge of $+100\,V_{pp}$, the influences can be reduced to 3.51 %. A deviation of -0.88 % can be observed for falling edges of the inverter output. Hence, by contacting the handle wafer, a reduction of the frequency change of 52.42 % and 77.35 % for the rising and falling edges, respectively, compared to floating handle wafer coupling were achieved (see Table 5.1).

Table 5.1.: Comparison of output frequency chances caused by inverter coupling and handle wafer voltage changes for changes of -50 V and +50 V for floating (see Table 4.3) and grounded handle wafer.

	HW floating		HW grounded	
	$f_{SSCG,peak}$ [MHz]	ϵ [%]	$f_{SSCG,peak}$ [MHz]	ϵ [%]
Rising edge	2.49	+7.37	2.39	+3.51
Falling edge	2.23	-3.88	2.29	-0.88

On the one hand, Figure 5.3 shows that the influences of ultra high voltage pulse generators on monolithically integrated mixed-signal circuits such as spread spectrum clock generators on thick SOI, are mainly caused by substrate coupling across the handle wafer. By applying a fixed potential to the handle wafer, the influences can be greatly reduced. On the other hand, Figure 5.3 also shows that other coupling



(a) Rising edge.

(b) Falling edge.

Figure 5.3.: Influences of the clock frequency f_{SSCG} of the spread spectrum clock generator with PRN = 1 for inverter output voltages of ±50 V and an output load of 1 nF. Interferences are reduced if the handle wafer is grounded.

mechanisms are present in the high voltage SOI circuit because the influences are not eliminated by grounding the handle wafer. This small proportion can be explained by inductive and capacitive couplings on the die, which were not taken into account by the post-layout simulations.

5.5 Summary

In summary it can be said that the effects of ultra high voltage pulse generators on components with low supply voltages can be reduced if some precautions are taken in the design phase of the high voltage integrated circuit. The technology selection has a significant impact on the influences between components with different voltage levels. While in bulk CMOS processes, regions with different voltage levels are separated by junction isolation allowing coupling across the substrate, the substrates of different components on the device wafer of SOI processes are completely separated by dielectric isolation.

Capacitive coupling of switching high voltage outputs to the handle wafer can occur. In n-substrate SOI processes these parasitic currents can couple on the supply voltage of the low voltage components. Therefore, it is important to stabilize these sufficiently with internal capacities and to make the connection of the substrates low impedance. Circuits with a high power supply rejection can further suppress the effects of parasitic coupling across the handle wafer.

The coupling via the handle wafer can be largely suppressed by applying a fixed potential on the handle wafer. If the process does not allow contacting the handle wafer on the die itself, the package has to be selected in a way that a rear contacting of the handle wafer is possible. During floorplanning, high voltage and low voltage components should be arranged with the greatest possible distance in between. Isolation structures such as dielectric isolation reduce the influences on the device wafer. The effects of

high voltage component dissipation on the chip have to be taken into account during implementation and packaging.

In the case of the fabricated example HVIC, it could be shown that an influence of the clock frequency of the implemented spread spectrum clock generator by the monolithic integrated three-state high voltage inverter can be completely prevented. For this purpose, the handle wafer of the SOI die was grounded, whereby switching cross currents were conducted to ground. Temperature-related influences could be counteracted by active cooling.

6 Conclusion

This thesis investigated the interference-aware integration of system-on-chips which include an ultra high voltage pulse generator and low voltage mixed-signal designs. A brief introduction to the various commercially available high voltage technologies was given. It was followed by an introduction to high voltage DMOS transistors and isolation techniques for components of different voltage domains. For high voltage integrated circuits with switching devices above 200 V, SOI-based technologies seemed to be most promising in terms of required chip area and cross talk between high voltage and low voltage building blocks. A three-state high voltage inverter capable of driving capacitive loads up to 10 nF such as pad-printed electroluminescent devices and ultrasound pulser was implemented in a 1 µm SOI BCD technology. It can deliver pulses of up to ±300 V at frequencies up to 5 kHz. A low voltage spread spectrum clock generator was implemented on the same SoC to excite capacitive sensors. It has a resolution of 9 bit, a bandwidth of 10.14 MHz and an attenuation of 33.17 dB and is powered by a 5 V power supply. With the help of the fabricated SoCs, the research questions of section 1.2 could be answered.

6.1 Conclusion

Implementing high voltage and low voltage components on the same chip was made possible by the expansion of More than Moore technologies. Thus, in addition to computing building blocks on an IC, power devices, sensor interfaces or RF components can be implemented on the same die resulting in a system-on-chip. By alternating use of the various components, these can be operated one after the other almost without interference. When operating ultra high voltage pulse generators at the same time along with mixed-signal designs such as the implemented SSCG, parasitic effects on the low voltage domain can be observed if no special precautions are taken.

In SOI based SoCs, three key influences can be observed. First, these are thermal influences by the power losses of the high voltage output stages. The thermal power dissipation of a high voltage pulse generator can be extracted by simulations with conventional tools. By knowing the packaging and the associated thermal resistance of the system, the chip temperature can be estimated prior to fabrication. Mixed-signal designs are therefore operated at higher temperatures.

Second, inductive and capacitive influences within the SoC are observed. Post-layout simulations can take into account some of these aspects. Designers of ultra high voltage pulse generators should implement shielding wires on ever metal layer between the high and low voltage components to prevent coupling effects.

Third, in SOI based SoCs, electrical coupling across the substrate handle wafer can occur. This is of special significance for switching high voltages with high amplitudes and slew rates. Charge can couple from the high voltage domain via the substrate to low voltage mixed-signal designs which can cause failures or even damage. Due to their structure, quasi-vertical n-channel DMOS transistors in n-wafers whose drains are connected to the switching output voltage are mainly responsible for the coupling. For high voltage output stages, the low-side transistor of output stages is a main source of substrate coupling.

Electrical couplings of the high voltage transients can be predicted by the substrate network and its automated extraction presented in this work. The substrate network is composed of the capacitance over the buried oxide and an RC-network of the handle wafer. The calculation of the values can be well

estimated without any fringing. More precise values are provided by TCAD simulations, from which a correction factor for the analytic calculation can be extracted. The information required by the layout of the IC can be extracted automatically with the help of a SKILL® based program. This can also create a substrate netlist, which is added to the actual circuit in post-layout simulations. For the implemented high voltage SoCs, the influences of an ultra high voltage pulse generator on the output frequency of a spread spectrum clock generator could be predicted using SPICE simulations in the conventional design flow.

From these investigations, design recommendations for the implementation of system-on-chips with an ultra high voltage pulse generator with high slew rates and amplitudes as well as monolithically integrated low voltage components were deduced. These include both technology-related and circuit-related considerations as well as aspects of packaging selection. Considering these aspects, interference-resistant system-on-chips with voltage pulses of ultra high amplitude and slew rates can be monolithically integrated along with low supply voltage mixed-signal designs to meet cost and complexity specifications.

6.2 Future Works

From the considerations of this work, an interesting question concerning the usability of the post-layout extraction for high voltage components arises. Inductive and capacitive coupling have to be considered for high voltage pulse generators. Since the design flow and the used tools were optimized for low voltage components, an extended range of influences might have to be considered for high voltage devices. Likewise, simulators could be extended for the special needs of high voltage designs reducing convergence problems during simulation.

In addition, the monolithic integration of high voltage and low voltage designs is mostly at the expense of the possibilities of low voltage implementation. Mixed-signal designs could usually be better implemented in different technologies. Processes with smaller structure sizes could be chosen, allowing faster circuits to be realized on smaller chip area. The manufactured and completely galvanically separated high voltage components and mixed-signal designs can be housed in one package, which is known as system-in-package. Influences between these dies would be a very interesting point for further consideration. Integrating the co-simulation of several chips of different technologies as well as the influence of the package in the conventional design flow would be another interesting starting point.

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A Commercially available Drivers for Electroluminescent Devices

Table A.1.: List of commercially available drivers for EL devices. Charge pump designs are marked in light blue. Except of HV809, HV850, HV852 and HV853 all other ICs are based on a boost converter with subsequent h-bridge.

Manufacturer	Manufacturer Number	V_{in} [V] min	V_{in} [V] max	V_{out} [V] min	V_{out} [V] max	f_{out} [Hz] min	f_{out} [Hz] max	C_{load} [nF] max
Microchip Technology	MIC4826	1.8	5.5	150	170	60	1000	
	MIC4827	1.8	5.5	166	194	60	1000	
	MIC4830	1.8	5.5	152	198	60	1000	
	MIC4832	1.8	5.5	182	218	60	1000	
	MIC4833	2.3	5.8	180	240	100	1500	
	MIC4834	2.3	5.8	180	240	165	285	
Supertex inc. / Microchip	HV809		210	100	400	100	1200	350
	HV816	2.7	5.5	320	400	100	1000	150
	HV823	2.0	9.2	160	200	330	450	
	HV825	1.0	1.6	104	124	400		6
	HV830	2.0	9.5	180	200		1500	
	HV833	1.8	6.5	160	200	60	1000	
	HV850	3.0	4.2	108	148	50	500	5
	HV852	2.4	5.0	144	184	50	500	5.3
	HV853	3.2	5.0	136	184	50	500	5.3
	HV857	1.8	5.0	170	210		1000	
	HV859	1.8	5.0	190	230	175	235	
	HV860	2.5	4.5	180	240	150	500	
	HV861	2.5	4.5	160	200	100	500	20
	HV881	1.8	5.5	290	390	200	1000	1
maxim Integrated	MAX14514	2.7	5.5	105	350	210	290	
	MAX14521E	2.7	5.5	66	320	194	424	
	MAX4990	2.5	5.5	84	280	210	290	
Monolithic Power Systems Inc.	MP3801	2.5	5.5	180	200	60	1000	
	MP3802	2.5	5.5			60	1000	

B Derivation of the Transconduction of the Voltage-to-Current Converter

The voltage-to-current converter of the implemented spread spectrum clock generator is explained in subsubsection 3.3.2.4. Its schematic is shown in Figure 3.32. The corresponding small signal equivalent circuit is shown in Figure 3.33.

In a first step, the input impedance of node N1 Z_{N1} is calculated for an open loop with

$$Z_{N1} = \frac{v_{N1}}{i_{C1}} \tag{B.1}$$

and

$$v_{N1} = i_{C1} Z_{C1} + i_{R2} Z_{R2}. \tag{B.2}$$

The current through resistor R_2 is given by

$$i_{R2} = i_{C1} + i_{out2+} = i_{C1} - x g_{m1}^* g_{m2}^* R_1 v_{N1}. \tag{B.3}$$

Inserting Equation B.3 and Equation B.2 in Equation B.1 results in

$$Z_{N1} = \frac{Z_{C1} + R_2}{1 + x g_{m1}^* g_{m2}^* R_1 R_2} = \frac{\frac{1}{sC_1} + R_2}{1 + x g_{m1}^* g_{m2}^* R_1 R_2}. \tag{B.4}$$

Since the input resistor R is large in size, an input capacitance C_{in} at node N1 can be assumed. Therefore, the overall input impedance at node N1 is

$$Z_{N1}^* = Z_{N1} || \frac{1}{sC_{in}} = \frac{R_2 + \frac{1}{sC_1}}{1 + x g_{m1}^* g_{m2}^* R_1 R_2} || \frac{1}{sC_{in}} \tag{B.5}$$

which equals Equation 3.18.

Second, the transconductance g_m^* of the current i_{C2} through capacitor C_2 to the voltage v_{N1} at node N1 is calculated by

$$g_m^* = \frac{i_{C2}}{v_{N1}}. \tag{B.6}$$

The current i_{C2} is given by

$$i_{C2} = i_{out2-} + i_{out3} \tag{B.7}$$

with

$$i_{out3} = -g_{m3}^* v_{N4} = -\frac{1}{xR_2} i_{R2} R_2 = \frac{-i_{R2}}{x}. \tag{B.8}$$

Inserting Equation B.1 and Equation B.3 in Equation B.8 results in

$$i_{\text{out3}} = v_{\text{N1}} \left(g^*_{\text{m1}} g^*_{\text{m2}} R_1 - \frac{1}{x Z_{\text{N1}}} \right). \tag{B.9}$$

Inserting Equation B.9 and

$$i_{\text{out2}-} = v_{\text{N1}} g^*_{\text{m1}} g^*_{\text{m2}} R_1 \tag{B.10}$$

in Equation B.7 and subsequently in Equation B.6 results in

$$g^*_{\text{m}} = \frac{i_{\text{C2}}}{v_{\text{N1}}} = 2 g^*_{\text{m1}} g^*_{\text{m2}} R_1 - \frac{\frac{1}{x} + g^*_{\text{m1}} g^*_{\text{m2}} R_1 R_2}{R_2 + \frac{1}{sC_1}} \tag{B.11}$$

which equals Equation 3.17. With these calculations, the small signal equivalent circuit can be simplified as shown in Figure B.1.

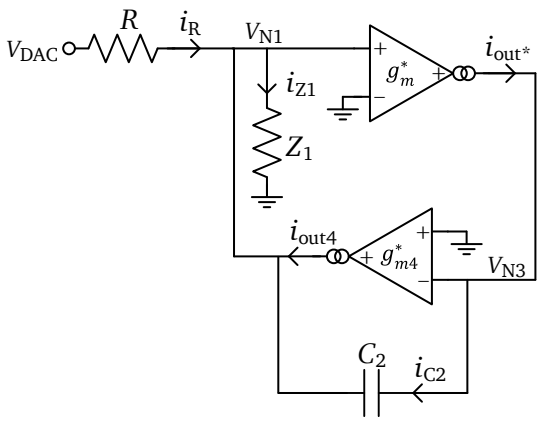

Figure B.1.: Compressed small signal equivalent circuit to derive the transconductance of the voltage to current converter.

In the third step, the transconductance of the overall voltage-to-current converter can be calculated by

$$g_{\text{V-I-converter}} = \frac{i_{\text{out4}}}{v_{\text{DAC}}}. \tag{B.12}$$

The output current i_{out4} is given by

$$i_{\text{out4}} = g^*_{\text{m4}} v_{\text{N3}}. \tag{B.13}$$

From Ohm's law it follows that the current i_{C2} in capacitor C_2 is given by

$$i_{\text{C2}} = (v_{\text{N3}} - v_{\text{N1}}) s C_2 \tag{B.14}$$

which can be transformed to

$$v_{\text{N3}} = \frac{i_{\text{C2}} + v_{\text{N1}} s C_2}{s C_2} = \frac{v_{\text{N1}} \left(g^*_{\text{m}} + s C_2 \right)}{s C_2} \tag{B.15}$$

by inserting

$$i_{\text{C2}} = i_{\text{out*}} = g^*_{\text{m}} v_{\text{N1}}. \tag{B.16}$$

Hence, the voltage at node N1 can be express as a function of the output current i_{out4} by inserting Equation B.15 in Equation B.13

$$v_{\mathrm{N1}} = \frac{i_{\mathrm{out4}} s C_2}{g^*_{\mathrm{m4}} \left(g^*_{\mathrm{m}} + s C_2 \right)} \tag{B.17}$$

From Kirchoff's current law it follows that

$$i_{\mathrm{out4}} + i_{\mathrm{C2}} + i_{\mathrm{R}} = i_{\mathrm{Z1}}. \tag{B.18}$$

With

$$i_{\mathrm{R}} = \frac{v_{\mathrm{DAC}} - v_{\mathrm{N1}}}{R} \tag{B.19}$$

and Equation B.16 as well as Equation B.17, i_{out4} can be expressed by the input voltage v_{DAC}. By transformation and deviation, the transconductance of the voltage-to-current converter can be extracted to

$$g_{\mathrm{V-I-converter}} = \frac{i_{\mathrm{out4}}}{v_{\mathrm{DAC}}} = \frac{g^*_{\mathrm{m4}} \left(g^*_{\mathrm{m}} + s C_2 \right)}{s C_2 Z^*_{\mathrm{N1}} + R \left(s C_2 + g^*_{\mathrm{m}} s C_2 Z^*_{\mathrm{N1}} + g^*_{\mathrm{m4}} s C_2 Z^*_{\mathrm{N1}} \right)} \tag{B.20}$$

which equals Equation 3.16. The parameters of the different stages are extracted from SPICE simulations as listed in Table B.1.

Table B.1.: Extracted small signal parameters of the voltage-to-current converter.

Parameter	Value
R	100.1 kΩ
R_1	40.0 kΩ
R_2	80.3 kΩ
C_1	300.0 fF
C_2	1.0 pF
g^*_{m1}	33.4 µS
g^*_{m2}	2.5 µS
g^*_{m4}	70.9 µS
C_{in}	400 fF
x	5

C SKILL® Code for Automated Extraction of the Substrate Network

The SKILL® code for the automated extraction of the substrate network is shown in this chapter. The following codes can be downloaded from the Cadence® support website:

- CCSsumAreas.il
- MaxWidth.il
- CCSCtPtPolygon.il
- CCSCreateWireForPin.il
  Has to be adapted so that library name and cell name can be transferred
  → CCSCreateWireForPin_adapted.il

```
; load("Substrate_Network_Wmax.il")

;; in layout:
;; PBULK=VDDa
;; DEPLD=VDDd
;; HWCNT=Vout_HV

;; procedure:
; 0. Definitions
; 1. calculate areas of all polygons in different layers
; 2. Calculate center of all polygons in different layers
; 3. insert capacitances and Resistance to HW for different areas (and connection to VDD/Vout_HV)
; 4. Calculate distances of all shapes of Vout_HV to all shapes of VDDa and VDDd respectively
; 5. Insert Resistances and Connections to capacitors

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; 0. Definitions ;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

signals=(list "Vout_HV" "VDDa" "VDDd")
layers=(list "HWCNT" "PBULK" "DEPLD")

CV_Lib="Substrate_Extraction"
CV_Cell="Substrate_DCO_TB"

xC=0
yC=0

xR=0
yR=-0.6 ; (direct connection to Cap if yR=-0.4)

epsilon_null=8.854187817e-12
epsilon_BOX=3.9
d_BOX=2; um
CPA_STHW=epsilon_null*epsilon_BOX*1e-6/d_BOX
;CPA_STHW=0.017*1e-15

rho=40000; Ohm*um
d_HW=570 ; um
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; 1. calculate areas of all polygons in different layers ;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

cv_layout = dbOpenCellViewByType(CV_Lib CV_Cell "layout" "" "r")

; get shapes
shape_Vout_HV=setof(shapes cv_layout~>shapes
member(shapes~>objType '("rect" "polygon")) &&
shapes~>layerName=="HWCNT") ;; change layer here

shape_VDDd=setof(shapes cv_layout~>shapes
member(shapes~>objType '("rect" "polygon")) &&
shapes~>layerName=="DEPLD") ;; change layer here

shape_VDDa=setof(shapes cv_layout~>shapes
member(shapes~>objType '("rect" "polygon")) &&
shapes~>layerName=="PBULK") ;; change layer here

load("CCSsumAreas.il")

area_Vout_HV=foreach( mapcar Vout_HVShape
shape_Vout_HV
CCScalcArea(Vout_HVShape))

area_VDDa=foreach( mapcar VDDaShape
shape_VDDa
CCScalcArea(VDDaShape))

area_VDDd=foreach( mapcar VDDdShape
shape_VDDd
CCScalcArea(VDDdShape))

;; Calculate maximum Width
load("MaxWidth.il")

wmax_Vout_HV_all=foreach( mapcar Vout_HVShape shape_Vout_HV
maxwidth(Vout_HVShape))

wmax_VDDa_all=foreach( mapcar VDDaShape shape_VDDa
maxwidth(VDDaShape))

wmax_VDDd_all=foreach( mapcar VDDdShape shape_VDDd
maxwidth(VDDdShape))
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; 2. Calculate center of all polygons in different layers ;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
load("CCSCtPtPolygon.il")

;; X-Coordinates
x_Vout_HV=foreach( mapcar Vout_HVShape
shape_Vout_HV
CCSCtPtx(Vout_HVShape))

x_VDDa=foreach( mapcar VDDaShape
shape_VDDa
CCSCtPtx(VDDaShape))

x_VDDd=foreach( mapcar VDDdShape
shape_VDDd
CCSCtPtx(VDDdShape))

;; Y-Coordinates
y_Vout_HV=foreach( mapcar Vout_HVShape
shape_Vout_HV
CCSCtPty(Vout_HVShape))

y_VDDa=foreach( mapcar VDDaShape
shape_VDDa
CCSCtPty(VDDaShape))

y_VDDd=foreach( mapcar VDDdShape
shape_VDDd
CCSCtPty(VDDdShape))


;; Save and Close Layout
;dbSave(cv_layout) ;; read-only Mode
dbClose(cv_layout)
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; 3. insert capacitances for different areas (and connection to VDD/Vout_HV) ;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; Open Schematic
cv_schematic = dbOpenCellViewByType(CV_Lib CV_Cell "schematic" "" "a")

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; Vout_HV
;; Place Cap and Res to Bottom of HW in Schematic
load("CCSCreateWireForPin_adapted.il")
(for i 1 length(area_Vout_HV)
;; get Area from list calculated by layout
n=i-1
A=(nth n area_Vout_HV)
;; Adaption of Capacitance
C=CPA_STHW*A
; Save value as string
C_CDF=aelSuffixNotation(C)
/* create Capacitance */
dbCreateParamInstByMasterName(cv_schematic "analogLib" "cap" "symbol" "" list(xC yC) "R0" 1
list(list("c" "string" C_CDF)));
/* Calculate Resistance */
R_HW=rho*d_HW/A
R_CDF=aelSuffixNotation(R_HW)
dbCreateParamInstByMasterName(cv_schematic "analogLib" "res" "symbol" "" list(xR yR) "R0" 1
list(list("r" "string" R_CDF)));
xC=xC+0.6
xR=xC

;; Connect MINUS pin of Cap and PLUS pin of Res to same Node
Pin_Name=strcat("HW_top_Vout_HV" sprintf(nil "CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res" "PLUS" Pin_Name)
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "cap"
"MINUS" Pin_Name)
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"PLUS" Pin_Name))

;; connect PLUS pin of capacitor to desired node ("Vout_HV"), MINUS pin of resistor to HW_bottom
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "res"
"MINUS" "HW_bottom")
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "cap"
"PLUS" "Vout_HV")
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "res"
"MINUS" "HW_bottom")
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; VDDa
;; Place Cap and Res to Bottom of HW in Schematic
(for i 1 length(area_VDDa)
;; get Area from list calculated by layout
n=i-1
A=(nth n area_VDDa)
;; Adaption of Capacitance
C=CPA_STHW*A
; Save value as string
C_CDF=aelSuffixNotation(C)
/* create Capacitance */
dbCreateParamInstByMasterName(cv_schematic "analogLib" "cap" "symbol" "" list(xC yC) "R0" 1
list(list("c" "string" C_CDF)));
/* Calculate Resistance */
R_HW=rho*d_HW/A
R_CDF=aelSuffixNotation(R_HW)
dbCreateParamInstByMasterName(cv_schematic "analogLib" "res" "symbol" "" list(xR yR) "R0" 1
list(list("r" "string" R_CDF)));
xC=xC+0.6
xR=xC

;; Connect MINUS pin of Cap and PLUS pin of Res to same Node
Pin_Name=strcat("HW_top_VDDa" sprintf(nil "CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"PLUS" Pin_Name)
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "cap"
"MINUS" Pin_Name)
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"PLUS" Pin_Name))

;; connect PLUS pin of capacitor to desired node ("VDDa"), MINUS pin of resistor to HW_bottom
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName
"res" "MINUS" "HW_bottom")
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName
"cap" "PLUS" "VDDa")
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName
"res" "MINUS" "HW_bottom")
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; VDDd
;; Place Cap and Res to Bottom of HW in Schematic
(for i 1 length(area_VDDd)
;; get Area from list calculated by layout
n=i-1
A=(nth n area_VDDd)
;; Adaption of Capacitance
C=CPA_STHW*A
; Save value as string
C_CDF=aelSuffixNotation(C)
/* create Capacitance */
dbCreateParamInstByMasterName(cv_schematic "analogLib" "cap" "symbol" "" list(xC yC) "R0" 1
list(list("c" "string" C_CDF)));
/* Calculate Resistance */
R_HW=rho*d_HW/A
R_CDF=aelSuffixNotation(R_HW)
dbCreateParamInstByMasterName(cv_schematic "analogLib" "res" "symbol" "" list(xR yR) "R0" 1
list(list("r" "string" R_CDF)));
xC=xC+0.6
xR=xC

;; Connect MINUS pin of Cap and PLUS pin of Res to same Node
Pin_Name=strcat("HW_top_VDDd" sprintf(nil "CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"PLUS" Pin_Name)
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "cap"
"MINUS" Pin_Name)
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"PLUS" Pin_Name))

;; connect PLUS pin of capacitor to desired node ("VDDd"), MINUS pin of resistor to HW_bottom
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"MINUS" "HW_bottom")
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "cap"
"PLUS" "VDDd")
CCSCreateWireForPin_adapted(cv_schematic~>
libName cv_schematic~>cellName "res"
"MINUS" "HW_bottom")
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; 4. Calculate distances of all shapes of Vout_HV to all shapes of VDDa and VDDd respectively ;;
; 5. Insert Resistances and Connections to capacitors
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; procedure
; 1. go through each element of Vout_HV (area/X-coordinates, y-ccordinates)
; 2. get x and y coordinates
; 3. go through each element of VDD
; 4. get x and y coordinates
; 5. calculate distance and resistance and insert it in schematic
; 6. connect to terminals of capacitors to HW_bottom
; 7. Repeat for other VDD

for(i_Vout_HV 1 length(area_Vout_HV)
n_Vout_HV=i_Vout_HV-1
xVout_HV=(nth n_Vout_HV x_Vout_HV)
yVout_HV=(nth n_Vout_HV y_Vout_HV)
wmax_Vout_HV=(nth n_Vout_HV wmax_Vout_HV_all)

; for VDDa
for(i_VDDa 1 length(area_VDDa)
n_VDDa=i_VDDa-1
xVDDa=(nth n_VDDa x_VDDa)
yVDDa=(nth n_VDDa y_VDDa)

wmax_VDDa=(nth n_VDDa wmax_VDDa_all)

distance_Vout_HV_VDDa=sqrt(abs((xVout_HV-xVDDa)* (xVout_HV-xVDDa)+(yVout_HV-yVDDa)*
(yVout_HV-yVDDa)))

; Calculate Resistance
; Mean Area
w_mean_VDDa=0.5*abs(wmax_Vout_HV-wmax_VDDa)
R_Vout_HV_VDDa=rho*distance_Vout_HV_VDDa/(d_HW*w_mean_VDDa)

; Insert Resistance
R_CDF_Vout_HV_VDDa=aelSuffixNotation(R_Vout_HV_VDDa)
dbCreateParamInstByMasterName(cv_schematic "analogLib" "res" "symbol" "" list(xR yR) "R0" 1
list( list("r" "string" R_CDF_Vout_HV_VDDa)));
xR=xR+0.6

; Connect Pins
Pin_Name_Vout_HV=strcat("HW_top_Vout_HV" sprintf(nil "Pin_Name_VDDa=
strcat("HW_top_VDDa" sprintf(nil "CCSCreateWireForPin_adapted(cv_schematic~>libName
cv_schematic~>cellName "res" "PLUS" Pin_Name_Vout_HV)
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "res"
"MINUS" Pin_Name_VDDa)
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "res"
"PLUS"
Pin_Name_Vout_HV)
```

```
) ;for VDDa


; for VDDd
for(i_VDDd 1 length(area_VDDd)
n_VDDd=i_VDDd-1
xVDDd=(nth n_VDDd x_VDDd)
yVDDd=(nth n_VDDd y_VDDd)

wmax_VDDd=(nth n_VDDd wmax_VDDd_all)

distance_Vout_HV_VDDd=sqrt(abs((xVout_HV-xVDDd)*
(xVout_HV-xVDDd)+(yVout_HV-yVDDd)*(yVout_HV-yVDDd)))

; Calculate Resistance)
; Mean Area
w_mean_VDDd=0.5*abs(wmax_Vout_HV-wmax_VDDd)
R_Vout_HV_VDDd=rho*distance_Vout_HV_VDDd/(d_HW*w_mean_VDDd)

; Insert Resistance
R_CDF_Vout_HV_VDDd=aelSuffixNotation(R_Vout_HV_VDDd)
dbCreateParamInstByMasterName(cv_schematic "analogLib" "res" "symbol" "" list(xR yR) "R0" 1 list(
list("r" "string" R_CDF_Vout_HV_VDDd)));
xR=xR+0.6

; Connect Pins
Pin_Name_Vout_HV= strcat("HW_top_Vout_HV" sprintf(nil "Pin_Name_VDDd=
strcat("HW_top_VDDd" sprintf(nil "CCSCreateWireForPin_adapted(cv_schematic~>libName
cv_schematic~>cellName "res"
"PLUS" Pin_Name_Vout_HV)
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "res"
"MINUS" Pin_Name_VDDd)
CCSCreateWireForPin_adapted(cv_schematic~>libName cv_schematic~>cellName "res"
"PLUS"
Pin_Name_Vout_HV)

) ;for VDDd

) ;for Vout_HV
```

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; END ;;
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;

;; Save and Close Schematic
;dbSave(cv_schematic)
dbClose(cv_schematic)
```

D Small Signal Equivalent Circuit of the Implemented Three-State High Voltage Inverter

The schematic of the implemented three-state high voltage inverter is shown in Figure 3.19. Its complete small signal equivalent circuit including the capacitances between gate and drain, gate and source as well as drain and source are included. For the simplified version shown in Figure 4.10, amongst others the transconductances are removed since the measurement was performed in subtreshold condition of the MOSFETs.

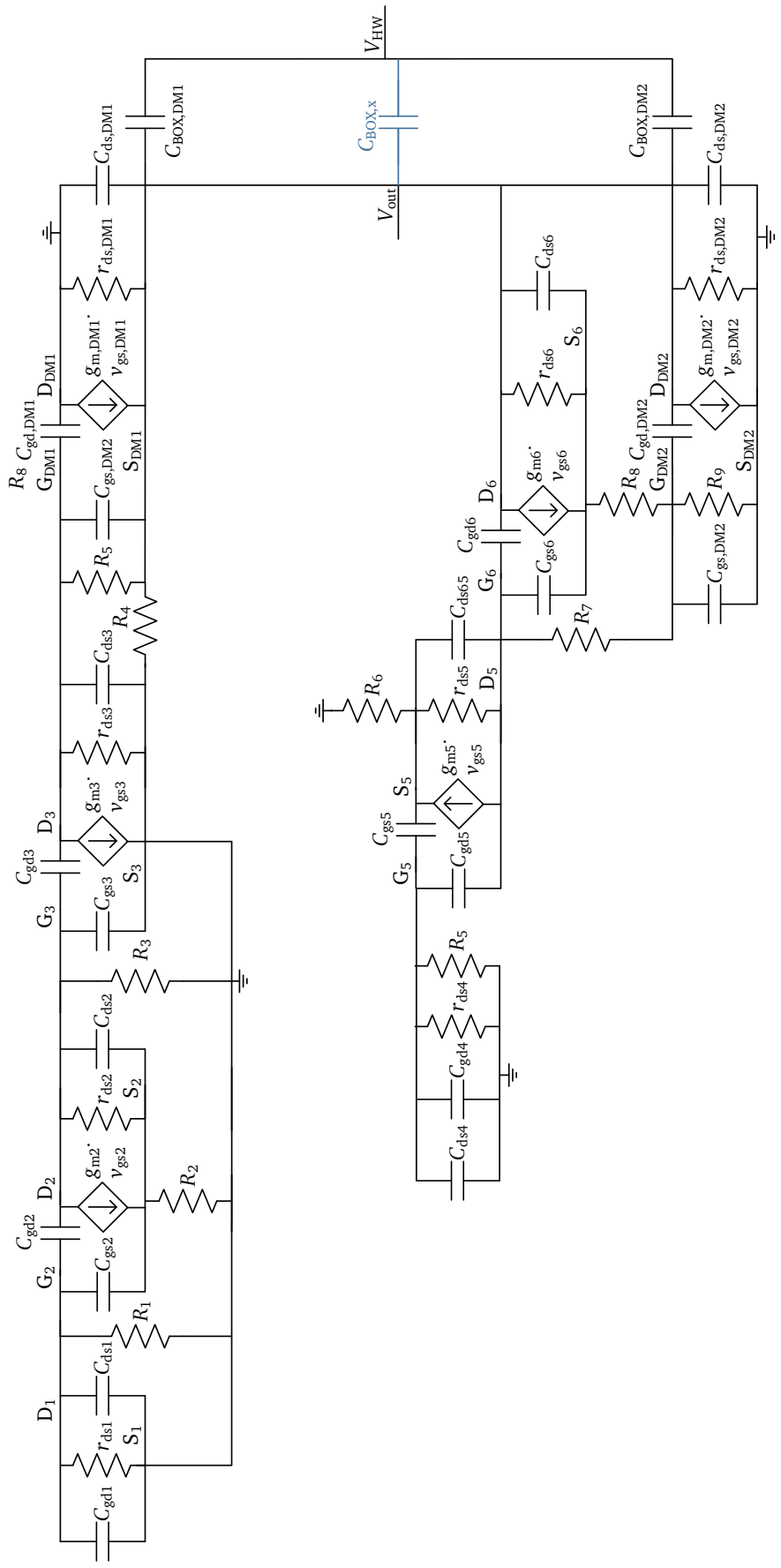

Figure D.1.: Small signal equivalent circuit of the implemented three-state high voltage inverter.

E Impedance Measurement of the Impedance between the Handle Wafer and the Output of the Inverter

The measurement of the impedance between the handle wafer and the output of the high voltage inverter was performed by a ModuLab®XM ECS system. So called Constant Level Impedance measurements were performed in sample and reference mode which calibrates the measured value with an internal reference. An alternating voltage is applied with frequencies from 10 Hz to 1 MHz. The amplitude was set to 0.1 V_{rms} to be below the threshold voltage of the high voltage DMOS transistors. A more detailed description of the measurement setup can be found in Figure 4.12 and in subsection 4.3.1.

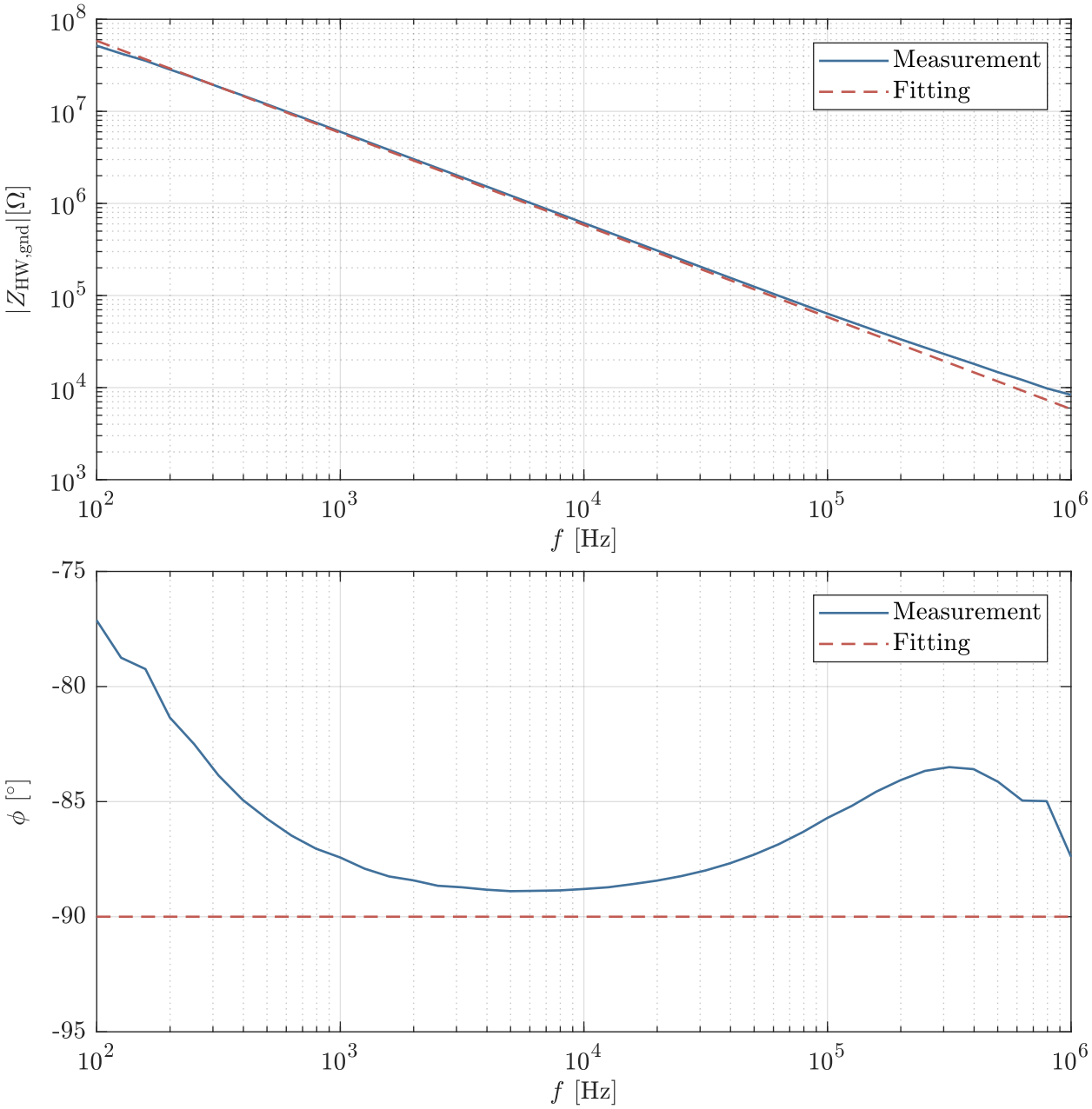

Figure E.1.: Bode plot of the impedance between the handle wafer and the output of the three-state high voltgae inverter $Z_{\mathrm{HW,gnd}}$. The generating signal was connected to the handle wafer. The measurement was performed with 0.1 V_{rms}.

Table E.1.: Fitting parameters for the impedance of the packages IC on the PCB. The impedance can be fitted with a capacitor for the required frequencies. Fitting method was calc-modulus.

Parameter	Value	Error
$C_{\mathrm{HW,gnd}}$	27.25 pF	0.021

F Impedance Measurements of the Handle Wafer Load

The impedance measurements were performed by a ModuLab®XM ECS system. So called Constant Level Impedance measurements were performed in sample and reference mode which calibrates the measured value with an internal reference. An alternating voltage is applied with frequencies from 10 Hz to 1 MHz. The amplitude is set with respect to the load and is noted in the sections below.

F.1 Impedance of the IC and Package

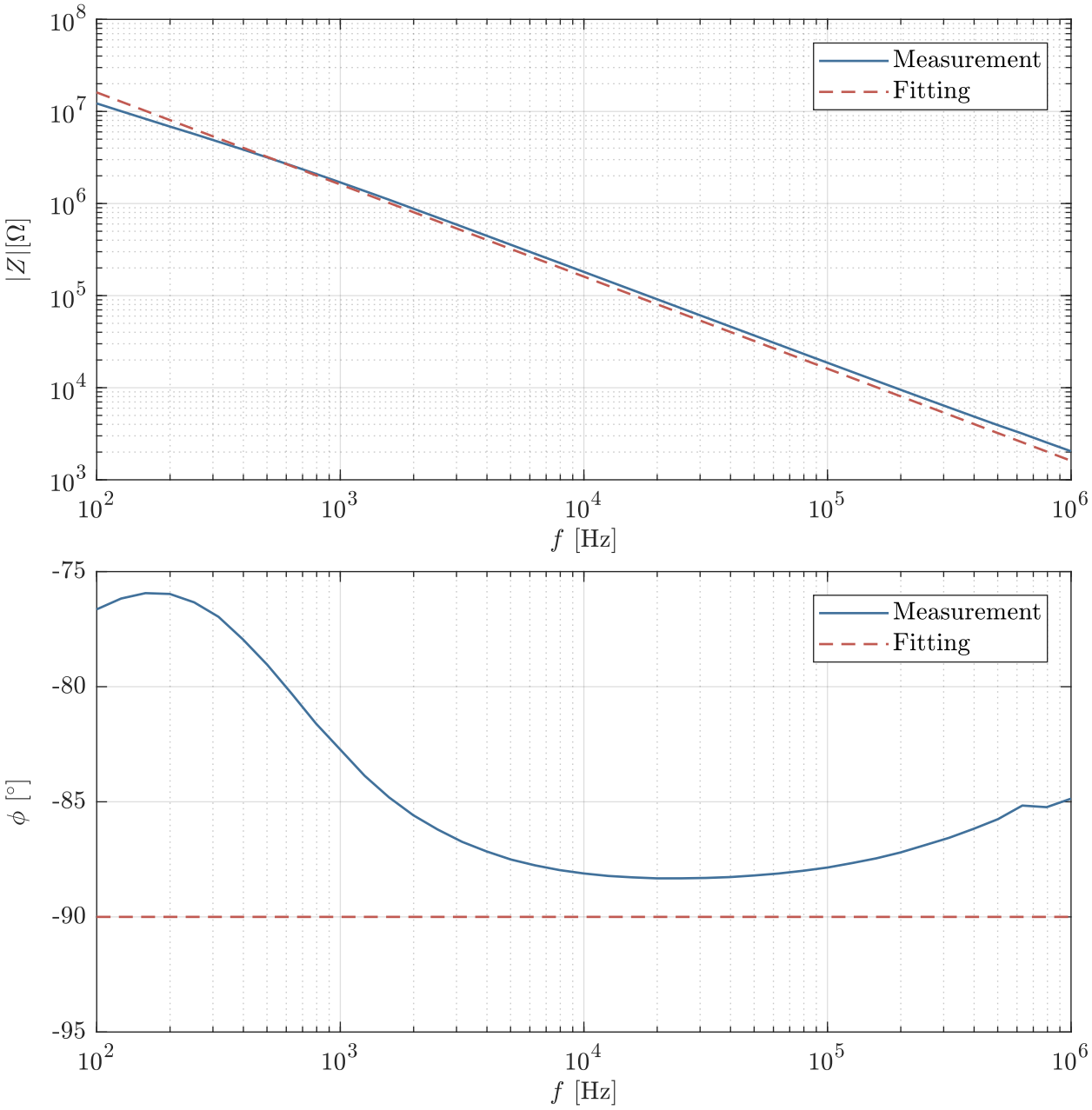

Figure F.1.: Bode plot of the impedance of the packages IC on the PCB. Measurement was performed with 2.5 V_{rms}.

Table F.1.: Fitting parameters for the impedance of the packages IC on the PCB. The probe can be fitted by a capacitor for the required frequencies. Fitting method was calc-modulus.

Parameter	Value	Error
C_{PCB}	98.88 pF	0.023

F.2 Impedance of the Probe

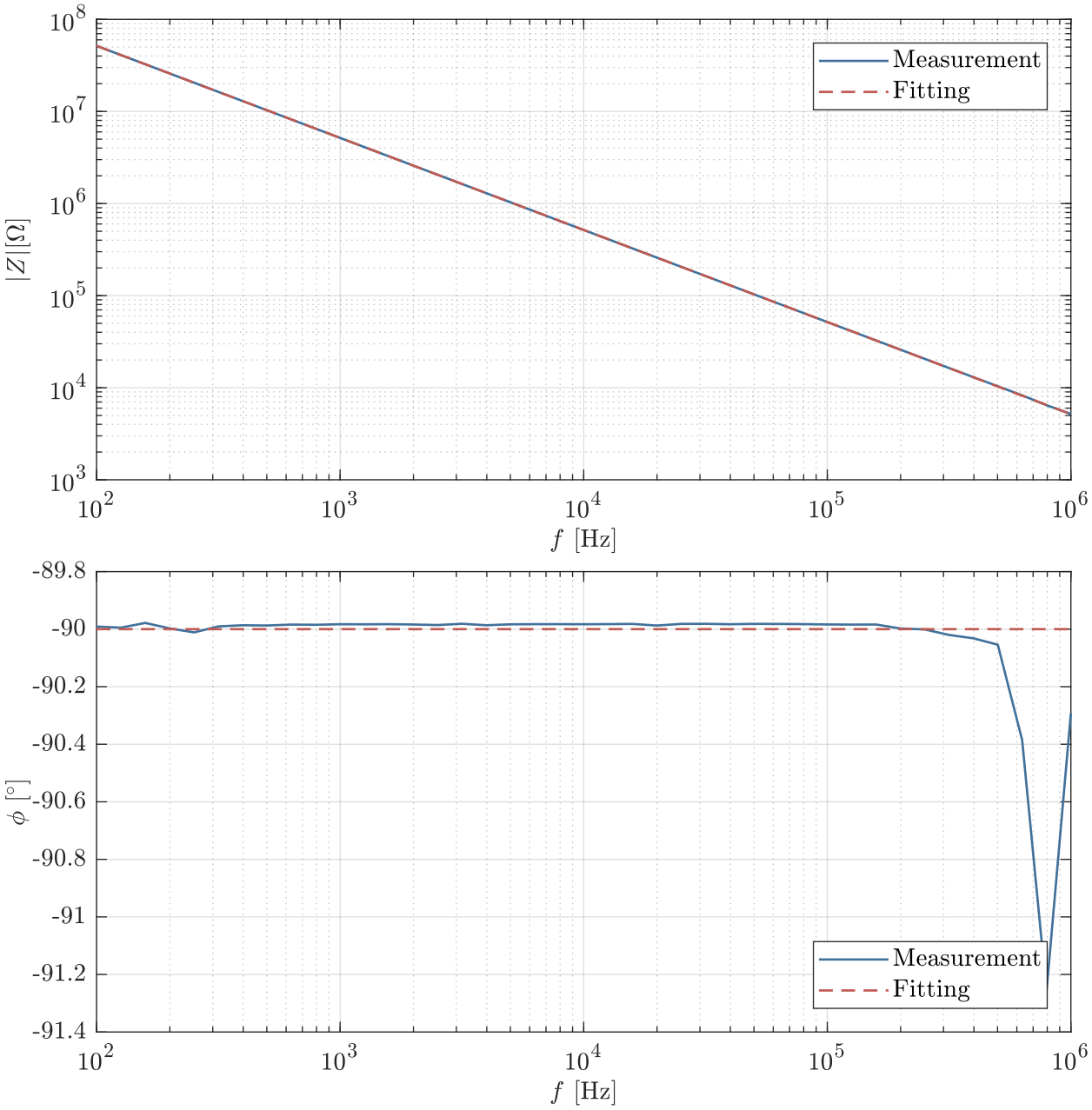

Figure F.2.: Bode plot of the impedance of the probe which contacted the handle wafer. Measurement was performed with 5 V_{rms}.

Table F.2.: Fitting parameters for the impedance of the probe which contacted the handle wafer. The probe can be fitted by a capacitor for the required frequencies. Fitting method was data-modulus.

Parameter	Value	Error
C_{probe}	30.82 pF	0.00039

F.3 Impedance of the BNC Cable

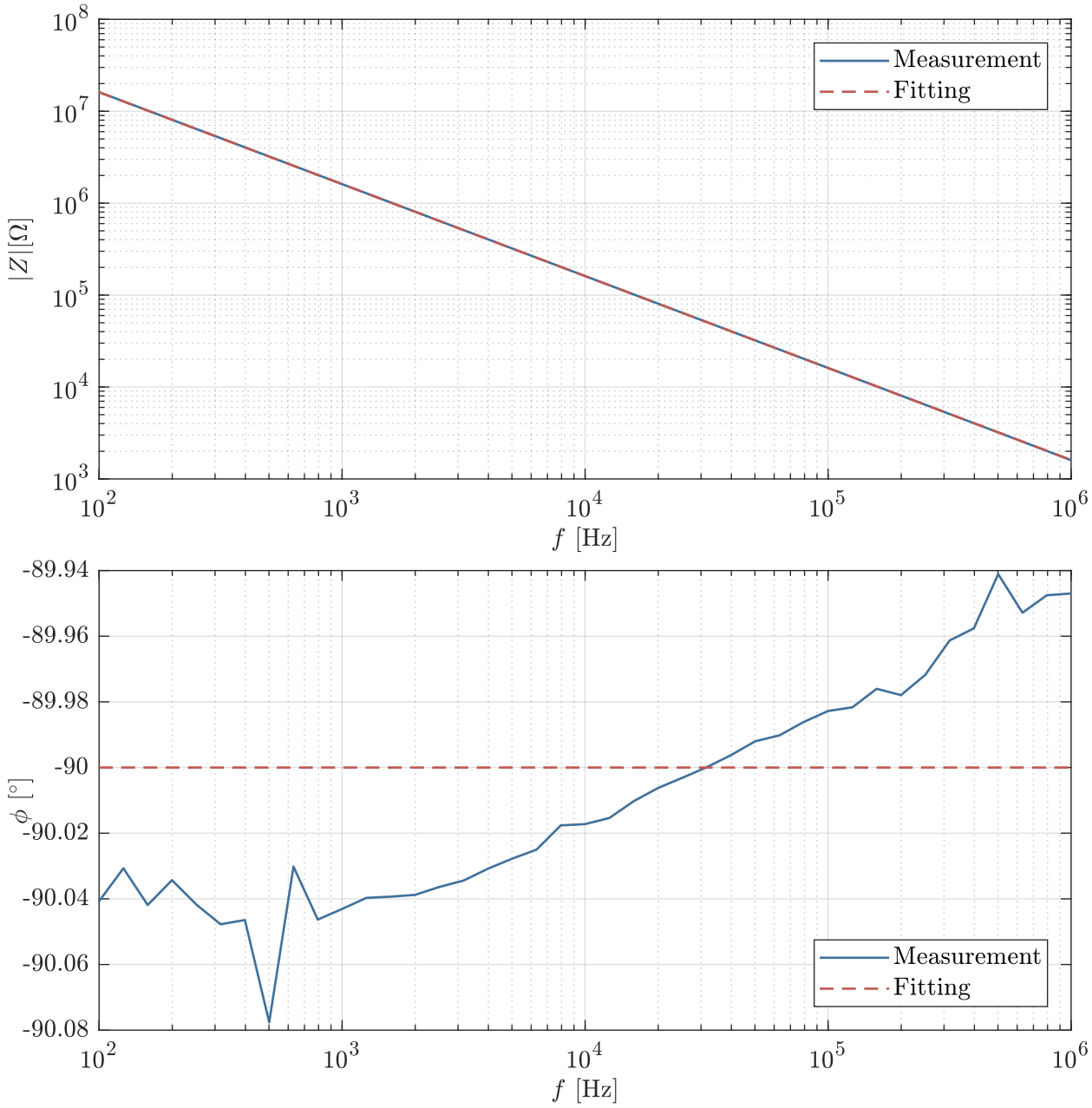

Figure F.3.: Bode plot of the impedance of the BNC cable used for the measurements at the handle wafer. Measurement was performed with 5 V_{rms}.

Table F.3.: Fitting parameters for the impedance of the BNC cable used for the measurements at the handle wafer. The BNC cable can be fitted by a capacitor for the required frequencies. Fitting method was data-modulus.

Parameter	Value	Error
C_{BNC}	98.82 pF	0.00079

F.4 Impedance of the Oscilloscope Tektronik TDS2024C

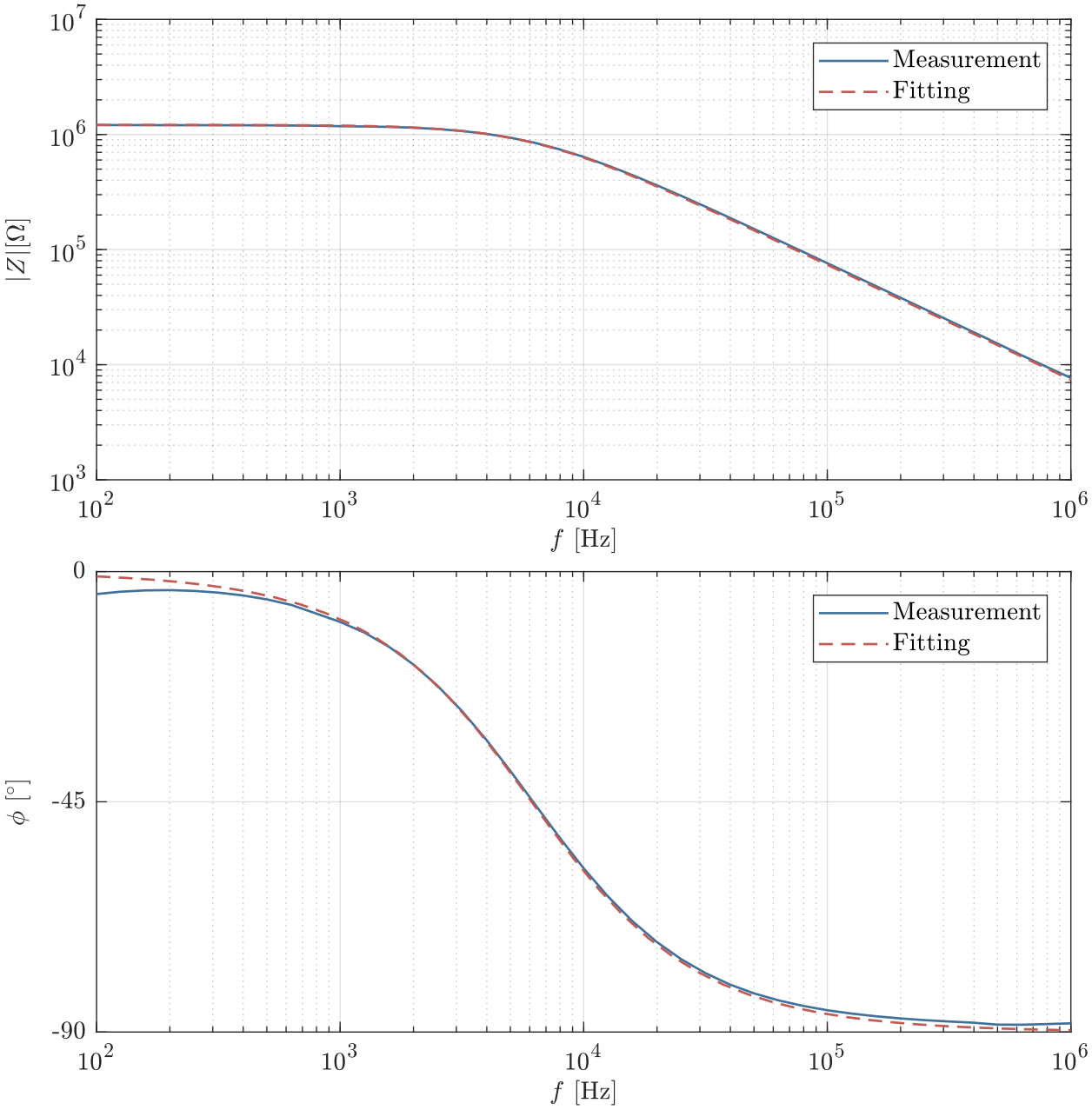

Figure F.4.: Bode plot of the input impedance of the oscilloscope Tektronik TDS2024C at 2.5 V_{rms}.

Table F.4.: Fitting parameters for the input impedance of the oscilloscope Tektronik TDS2024C at 2.5 V_{rms}. The equivalent circuit is a parallel connection of a capacitor and a resistor. Fitting method was data-modulus.

Parameter	Value	Error
C_{scope}	21.53 pF	0.065
R_{scope}	1.21 MΩ	0.019

List of Own Publications

[132] K. Hirmer and K. Hofmann, "Predicting Interferences of Switching High Voltage Devices on Mixed-Signal Designs," 2019, accepted for publication at the *26th IEEE International Conference on Electronics Circuits and Systems (ICECS)*.

[133] K. Hirmer, T. Casper, S. Schöps, and K. Hofmann, "3D Field Simulation Model for Bond Wire On-Chip Inductors Validated by Measurements," 2019, accepted for publication at the *Kleinheubacher Tagung 2019*.

[134] K. Hirmer, C. Bodenstein, H. M. Sauer, E. Dörsam, and K. Hofmann, "Nonlinear Behavior in Electrical Properties of Fully Screen Printed Electroluminescent Panels," accepted for publication at the *Journal of Print and Media Technology Research (JPMTR)*. DOI: 10.14622/JPMTR-1905.

[135] K. Hirmer and K. Hofmann, "Substrate Coupling in a Fully Integrated Three-State High Voltage Inverter," in *17th IEEE International NEWCAS Conference in Munich*. IEEE, 2019.

[136] C. Bodenstein, H. M. Sauer, K. Hirmer, and E. Dörsam, "Printing process and characterization of fully pad printed electroluminescent panels on curved surfaces," *Journal of Coatings Technology and Research*, Jul 2019. DOI: 10.1007/s11998-019-00243-0

[137] K. Hirmer, M. B. Saif, and K. Hofmann, "Integrated Symmetrical High-voltage Inverter for the Excitation of Touch Sensitive Electroluminescent Devices," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*. IEEE, 2018. DOI: 10.1109/ISPSD.2018.8393673 pp. 343–346.

[138] C. Bodenstein, H. M. Sauer, E. Dörsam, and K. Hirmer, "Influence of Printing Parameters in Fully Pad-printed Electroluminescence Panels on Curved Surfaces," in *19th International Coating Science and Technology Symposium*, 2018.

[139] K. Hirmer, D. Korner, and K. Hofmann, "Improving the Efficiency of a Multistage Boost Converter with Parallel Inductor Charging," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2018. DOI: 10.1109/COMPEL.2018.8459928 pp. 1–6.

[140] K. Hirmer, P. Schuster, F. Keil, and K. Hofmann, "Low-cost High-voltage Arbitrary Waveform Generator for Broad Lifetime Measurements of Electroluminescent Devices," in *Power Electronics Conference (SPEC), IEEE Annual Southern*. IEEE, 2016. DOI: 10.1109/SPEC.2016.7846014 pp. 1–4.

[141] L. Shen, K. Schaechtle, C. Küller, and K. Hofmann, "Hochintegration von Ladungspumpenarchitekturen in Hochvolt-CMOS-Technologien," in *Tagungsband der 14. ITG/GMM-Fachtagung Analog 2014*, 2014, pp. 1–6.

Supervised Theses

[142] F. C. Fink, “Kapazitive Sensoren —Funktionsweise und Auswertemethoden,” Bachelor’s thesis, 2014.

[143] T. Yuzkiv, “Auswertemethoden kapazitiver Näherungssensoren,” Bachelor’s seminar, 2014.

[144] P. Schuster, “Design and Implementation of a High Voltage Signal Generator for the Excitation of Electroluminescent Devices,” Master’s thesis, Technische Universität Darmstadt, 2015.

[145] F. C. Fink, “Implementierungen einer Über- und Unterspannungsabschaltung in einem 0,18 μm SOI-Prozess,” Bachelor’s thesis, 2016.

[146] T. de Oliveira Schneider, “Analyse eines Hochvolt-Signalgenerators zur Detektion von Schwachstellen,” Bachelor’s seminar, 2016.

[147] ——, “Verbesserung der Ausfallsicherheit eines Hochvolt-Signalgenerators durch Anpassung der Hochvolt-Ausgangsstufe,” Student research project, 2017.

[148] K. Kunst, “Kontaktlose Energieübertragung mittels Induktion zur Spannungsversorgung eines EL-Device,” Bachelor’s seminar, 2017.

[149] D. Korner, “Increasing Efficiency for Multi Stage Boost Converter,” Master’s seminar, 2017.

[150] F. Schopp, “Analysis of different over current protection principles and their adaption for high Voltage,” Student research project, 2017.

[151] C. Heinz, “Implementation of a Capacitive Sensor Readout using Analog and Digital Signal Processing,” Master’s seminar, 2017.

[152] D. Riehl, “3D Field Simulation Model for Bondwire On-Chip Inductors Validated by Measurements,” Master’s seminar, 2018.

[153] I. Kargar, “3D Field Simulation Model for Bondwire On-Chip Inductors Validated by Measurements,” Master’s seminar, 2018.

[154] D. Korner, “Implementation of an Integrated High-Voltage Inverter using an Area-efficient Charge Pump,” Master’s thesis, Technische Universität Darmstadt, 2018.

[155] T. Oster, “Entwicklung eines Spread-Spectrum-Oszillators in UMC65-Technologie,” Master’s seminar, 2018.

[156] R. Koch, “Reliability Aware Design in Smart Power Integrated Circuits,” Master’s seminar, 2019.